

# SHT32F21

## RAM Mapping 32×4 LCD Controller

### Features

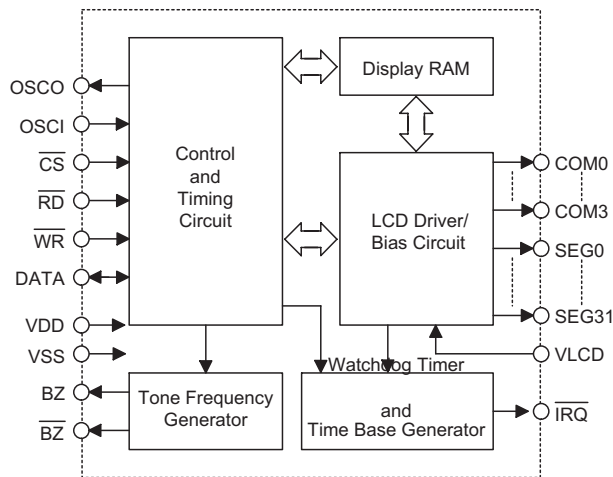
- Operating voltage: 2.4V~5.2V
- Built-in 256kHz RC oscillator
- External 32.768kHz crystal or 256kHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2kHz/4kHz)
- Power down command reduces power consumption
- Built-in time base generator and WDT
- Time base or WDT overflow output
- 8 kinds of time base/WDT clock sources
- 32×4 LCD driver
- Built-in 32×4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- R/W address auto increment
- Three data accessing modes
- VLCD pin for adjusting LCD operating voltage
- SHT32F21: 48-pin SSOP package
- ~~SHT28D21: 28-pin SOP package~~
- SHT24F21: 24-pin SOP package

### General Description

The SHT32F21 is a 128 pattern (32×4), memory mapping, and multi-function LCD driver. The S/W configuration feature of the SHT32F21 makes it suitable for multiple LCD applications including LCD modules and display sub-

systems. Only three or four lines are required for the interface between the host controller and the SHT32F21. The SHT32F21 contains a power down command to reduce power consumption.

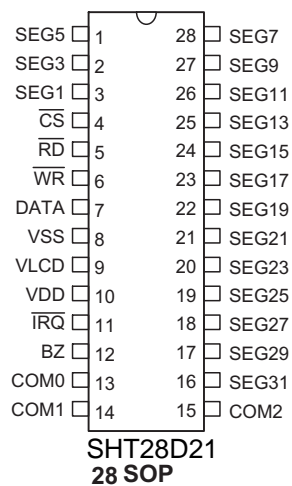
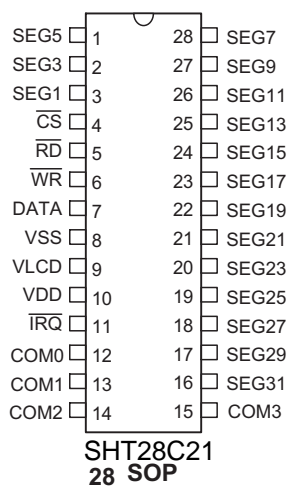
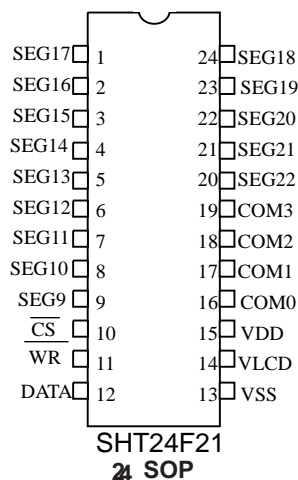
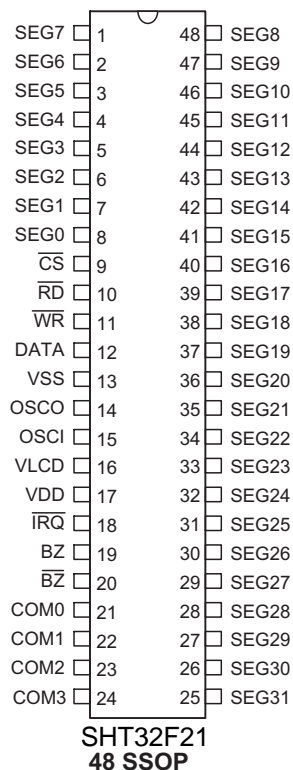
### Block Diagram



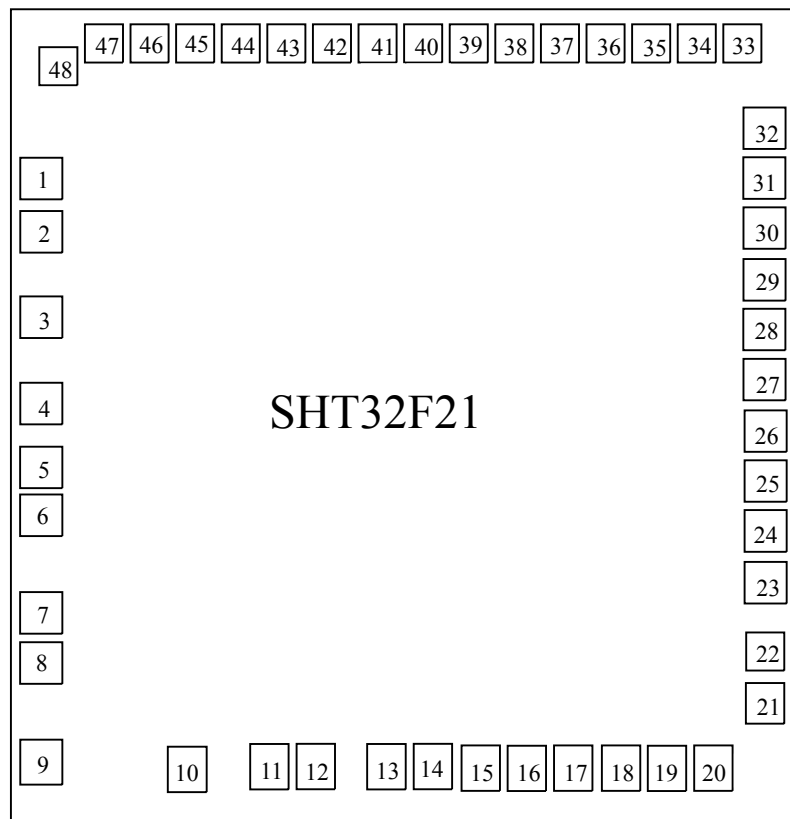
Note: CS: Chip selection  
BZ, BZ: Tone outputs  
WR, RD, DATA: Serial interface  
COM0~COM3, SEG0~SEG31: LCD outputs  
IRQ: Time base or WDT overflow output

## RAM Mapping 32×4 LCD Controller

### Pin Assignment



## RAM Mapping 32×4 LCD Controller



(0, 0)

PAD	NAME	X坐标	Y坐标	PAD	NAME	X坐标	Y坐标	PAD	NAME	X坐标	Y坐标
1	$\overline{\text{CS}}$	68	1515	17	SEG31	1514	67	33	SEG15	1915	1811
2	$\overline{\text{RD}}$	68	1387	18	SEG30	1634	67	34	SEG14	1795	1811
3	$\overline{\text{WR}}$	68	1128	19	SEG29	1754	67	35	SEG13	1675	1811
4	DATA	68	923.5	20	SEG28	1874	67	36	SEG12	1555	1811
5	VSS	68	762	21	SEG27	1947	262	37	SEG11	1435	1811
6	OSCO	68	642.5	22	SEG26	1947	382	38	SEG10	1315	1811
7	OSCI	68	385	23	SEG25	1947	532	39	SEG9	1195	1811
8	VLCD	68	265	24	SEG24	1947	652	40	SEG8	1075	1811
9	VDD	68	69	25	SEG23	1947	772	41	SEG7	955	1811
10	$\overline{\text{IRQ}}$	548	67	26	SEG22	1947	892	42	SEG6	835	1811
11	BZ	745.5	67	27	SEG21	1947	1012	43	SEG5	715	1811
12	BZ	858	67	28	SEG20	1947	1132	44	SEG4	595	1811
13	COM0	1034	67	29	SEG19	1947	1252	45	SEG3	475	1811
14	COM1	1154	67	30	SEG18	1947	1372	46	SEG2	355	1811
15	COM2	1274	67	31	SEG17	1947	1492	47	SEG1	235	1811
16	COM3	1394	67	32	SEG16	1947	1612	48	SEG0	115	1775

PAD坐标(X,Y)取PAD中心点,IC以左下角为坐标原点

\* The IC substrate should be connected to VDD in the PCB layout artwork.

## RAM Mapping 32×4 LCD Controller

### Pad Description

Pad No.	Pad Name	I/O	Function
1	$\overline{CS}$	I	Chip selection input with pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the SHT32F21 are disabled. The serial interface circuit is also reset. But if $\overline{CS}$ is at logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the SHT32F21 are all enabled.
2	$\overline{RD}$	I	READ clock input with pull-high resistor Data in the RAM of the SHT32F21 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with pull-high resistor Data on the DATA line are latched into the SHT32F21 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input/output with pull-high resistor
5	VSS	—	Negative power supply, ground
7	OSCI	I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
6	OSCO	O	
8	VLCD	I	LCD power input
9	VDD	—	Positive power supply
10	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output
11, 12	BZ, $\overline{BZ}$	O	2kHz or 4kHz tone frequency output pair
13~16	COM0~COM3	O	LCD common outputs
48~17	SEG0~SEG31	O	LCD segment outputs

VLCD

# RAM Mapping 32×4 LCD Controller

## Absolute Maximum Ratings

Supply Voltage ..... $V_{SS}-0.3V$  to  $V_{SS}+5.5V$       Storage Temperature ..... $-50^{\circ}C$  to  $125^{\circ}C$   
 Input Voltage ..... $V_{SS}-0.3V$  to  $V_{DD}+0.3V$       Operating Temperature ..... $-40^{\circ}C$  to  $85^{\circ}C$

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## D.C. Characteristics

$T_a=25^{\circ}C$

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		$V_{DD}$	Conditions				
$V_{DD}$	Operating Voltage	—	—	2.4	—	5.2	V
$I_{DD1}$	Operating Current	3V	No load/LCD ON	—	150	300	$\mu A$
		5V	On-chip RC oscillator	—	300	600	$\mu A$
$I_{DD2}$	Operating Current	3V	No load/LCD ON	—	60	120	$\mu A$
		5V	Crystal oscillator	—	120	240	$\mu A$
$I_{DD3}$	Operating Current	3V	No load/LCD ON	—	100	200	$\mu A$
		5V	External clock source	—	200	400	$\mu A$
$I_{STB}$	Standby Current	3V	No load, Power down mode	—	0.1	5	$\mu A$
		5V		—	0.3	10	$\mu A$
$V_{IL}$	Input Low Voltage	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
$V_{IH}$	Input High Voltage	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
$I_{OL1}$	DATA, BZ, $\overline{BZ}$ , $\overline{IRQ}$	3V	$V_{OL}=0.3V$	0.5	1.2	—	mA
		5V	$V_{OL}=0.5V$	1.3	2.6	—	mA
$I_{OH1}$	DATA, BZ, $\overline{BZ}$	3V	$V_{OH}=2.7V$	-0.4	-0.8	—	mA
		5V	$V_{OH}=4.5V$	-0.9	-1.8	—	mA
$I_{OL2}$	LCD Common Sink Current	3V	$V_{OL}=0.3V$	150	150	—	$\mu A$
		5V	$V_{OL}=0.5V$	150	250	—	$\mu A$
$I_{OH2}$	LCD Common Source Current	3V	$V_{OH}=2.7V$	-80	-120	—	$\mu A$
		5V	$V_{OH}=4.5V$	-120	-200	—	$\mu A$
$I_{OL3}$	LCD Segment Sink Current	3V	$V_{OL}=0.3V$	60	120	—	$\mu A$
		5V	$V_{OL}=0.5V$	120	200	—	$\mu A$
$I_{OH3}$	LCD Segment Source Current	3V	$V_{OH}=2.7V$	-40	-70	—	$\mu A$
		5V	$V_{OH}=4.5V$	-70	-100	—	$\mu A$
$R_{PH}$	Pull-high Resistor	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	60	120	200	k $\Omega$
		5V		30	60	100	k $\Omega$

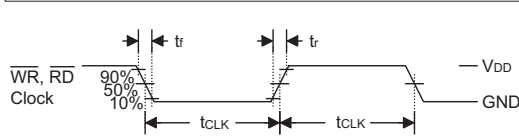
上海毅钧商贸有限公司 地址:上海市徐汇区小木桥路518弄2号1903室 邮编:200030  
 电话:021-54961838 传真:021-64035806 Email:ic108@ic108.com www.ic108.cn

**A.C. Characteristics**

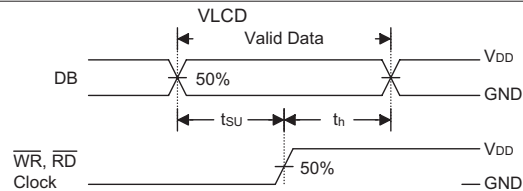
**RAM Mapping 32×4 LCD Controller**

Ta=25°C

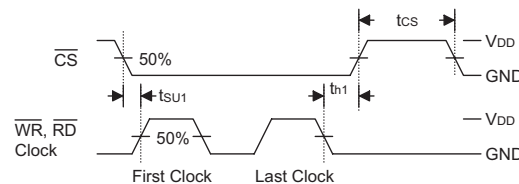
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
f <sub>SYS1</sub>	System Clock	—	On-chip RC oscillator	—	256	—	kHz
f <sub>SYS2</sub>	System Clock	—	Crystal oscillator	—	32.768	—	kHz
f <sub>SYS3</sub>	System Clock	—	External clock source	—	256	—	kHz
f <sub>LCD</sub>	LCD Clock	—	On-chip RC oscillator	—	f <sub>SYS1</sub> /1024	—	Hz
		—	Crystal oscillator	—	f <sub>SYS2</sub> /128	—	Hz
		—	External clock source	—	f <sub>SYS3</sub> /1024	—	Hz
t <sub>COM</sub>	LCD Common Period	—	n: Number of COM	—	n/f <sub>LCD</sub>	—	s
f <sub>CLK1</sub>	Serial Data Clock ( $\overline{WR}$ pin)	3V	Duty cycle 50%	4	—	150	kHz
		5V		4	—	300	kHz
f <sub>CLK2</sub>	Serial Data Clock ( $\overline{RD}$ pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	kHz
f <sub>TONE</sub>	Tone Frequency	—	On-chip RC oscillator	—	2.0 or 4.0	—	kHz
t <sub>CS</sub>	Serial Interface Reset Pulse Width (Figure 3)	—	$\overline{CS}$	—	250	—	ns
t <sub>CLK</sub>	$\overline{WR}$ , $\overline{RD}$ Input Pulse Width (Figure 1)	3V	Write mode	3.34	—	125	μs
			Read mode	6.67	—	—	
		5V	Write mode	1.67	—	125	μs
			Read mode	3.34	—	—	
t <sub>r</sub> , t <sub>f</sub>	Rise/Fall Time Serial Data Clock Width (Figure 1)	—	—	—	120	—	ns
t <sub>su</sub>	Setup Time for DATA to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 2)	—	—	—	120	—	ns
t <sub>h</sub>	Hold Time for DATA to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 2)	—	—	—	120	—	ns
t <sub>su1</sub>	Setup Time for $\overline{CS}$ to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 3)	—	—	—	100	—	ns
t <sub>h1</sub>	Hold Time for $\overline{CS}$ to $\overline{WR}$ , $\overline{RD}$ Clock Width (Figure 3)	—	—	—	100	—	ns



**Figure 1**



**Figure 2**



**Figure 3**

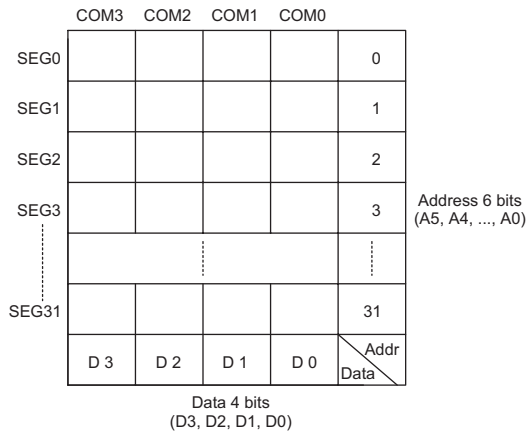
上海毅钧商贸有限公司 地址:上海市徐汇区小木桥路518弄2号1903室 邮编:200030  
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# RAM Mapping 32×4 LCD Controller

## Functional Description

### Display Memory – RAM

The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:



**RAM Mapping**

### System Oscillator

The SHT32F21 system clock is used to generate the time base/Watchdog Timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS

command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSC1 pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the SHT32F21 is at the SYS DIS state.

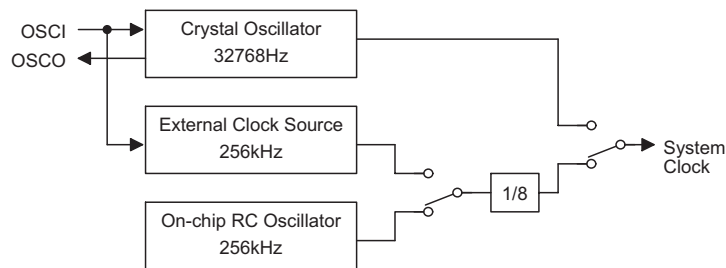
### Time Base and Watchdog Timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the  $\overline{\text{IRQ}}$  output by a command option. There are totally eight frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

$$f_{\text{WDT}} = \frac{32\text{kHz}}{2^n}$$

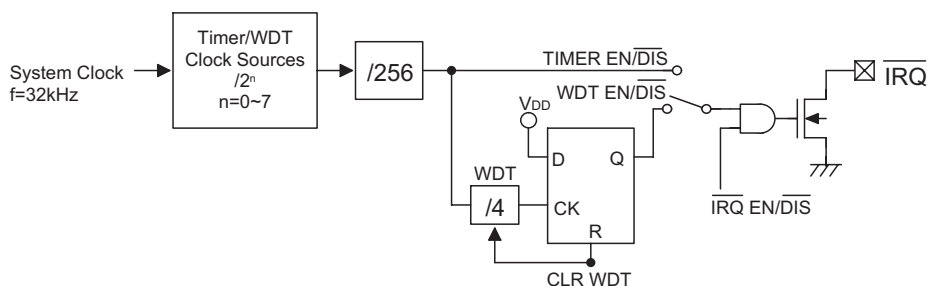
where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz.

If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands, one should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command



**System Oscillator Configuration**

## RAM Mapping 32×4 LCD Controller



### Timer and WDT Configurations

not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the  $\overline{\text{IRQ}}$  pin). After the **TIMER EN** command is transferred, the WDT is disconnected from the  $\overline{\text{IRQ}}$  pin, and the output of the time base generator is connected to the  $\overline{\text{IRQ}}$  pin. The WDT can be cleared by executing the **CLR WDT** command, and the contents of the time base generator is cleared by executing the **CLR WDT** or the **CLR TIMER** command. The **CLR WDT** or the **CLR TIMER** command should be executed prior to the **WDT EN** or the **TIMER EN** command respectively. Before executing the  $\overline{\text{IRQ}}$  EN command the **CLR WDT** or **CLR TIMER** command should be executed first. The **CLR TIMER** command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the  $\overline{\text{IRQ}}$  pin will stay at a logic low level until the **CLR WDT** or the  $\overline{\text{IRQ}}$  DIS command is issued. After the  $\overline{\text{IRQ}}$  output is disabled the  $\overline{\text{IRQ}}$  pin will remain at the floating state. The  $\overline{\text{IRQ}}$  output can be enabled or disabled by executing the  $\overline{\text{IRQ}}$  EN or the  $\overline{\text{IRQ}}$  DIS command, respectively. The  $\overline{\text{IRQ}}$  EN makes the output of the time base generator or of the WDT time-out flag appear on the  $\overline{\text{IRQ}}$  pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the corresponding system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the **SYS DIS** command turns out invalid and the power down mode fails to be carried out. That is, after the external clock source is selected, the SHT32F21 will continue working until system

power fails or the external clock source is removed. After the system power on, the  $\overline{\text{IRQ}}$  will be disabled.

### Tone Output

A simple tone generator is implemented in the SHT32F21. The tone generator can output a pair of differential driving signals on the **BZ** and **BZ**, which are used to generate a single tone. By executing the **TONE4K** and **TONE2K** commands there are two tone frequency outputs selectable. The **TONE4K** and **TONE2K** commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the **TONE ON** or the **TONE OFF** command. The tone outputs, namely **BZ** and **BZ**, are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the **BZ** and the **BZ** outputs will remain at low level.

### LCD Driver

The SHT32F21 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the **S/W** configuration. This feature makes the SHT32F21 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz even when it is at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

VLCD

The bold form of 1 0 0, namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command, will be omitted. The **LCD OFF** command turns the LCD display off by disabling the LCD bias gen-

Name	Command Code	Function
LCD OFF	<b>1 0 0</b> 0 0 0 0 0 1 0 X	Turn off LCD outputs VLCD
LCD ON	<b>1 0 0</b> 0 0 0 0 0 1 1 X	Turn on LCD outputs
BIAS & COM	<b>1 0 0</b> 0 1 0 a b X c X	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option VLCD

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## RAM Mapping 32×4 LCD Controller

erator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS and COM are the LCD panel related commands. Using the LCD related commands, the SHT32F21 can be compatible with most types of LCD panels.

### Command Format

The SHT32F21 can be configured by the S/W setting. There are two mode commands to configure the SHT32F21 resources and to transfer the LCD display data. The configuration mode of the SHT32F21 is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, a LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
Read	Data	1 1 0
Write	Data	1 0 1
Read-Modify-Write	Data	1 0 1
Command	Command	1 0 0

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the  $\overline{CS}$  pin should be set to "1" and the previous operation mode will be reset also. Once the  $\overline{CS}$  pin returns to "0" a new operation mode ID should be issued first.

### Interfacing

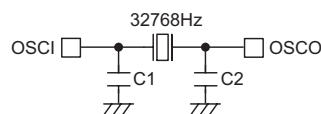
Only four lines are required to interface with the SHT32F21. The  $\overline{CS}$  line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the SHT32F21. If the  $\overline{CS}$  pin is set to 1,

the data and command issued between the host controller and the SHT32F21 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the SHT32F21. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The  $\overline{RD}$  line is the READ clock input. Data in the RAM are clocked out on the falling edge of the  $\overline{RD}$  signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the  $\overline{RD}$  signal. The  $\overline{WR}$  line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the SHT32F21 on the rising edge of the  $\overline{WR}$  signal. There is an optional  $\overline{IRQ}$  line to be used as an interface between the host controller and the SHT32F21. The  $\overline{IRQ}$  pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the  $\overline{IRQ}$  pin of the SHT32F21.

### Crystal Selection

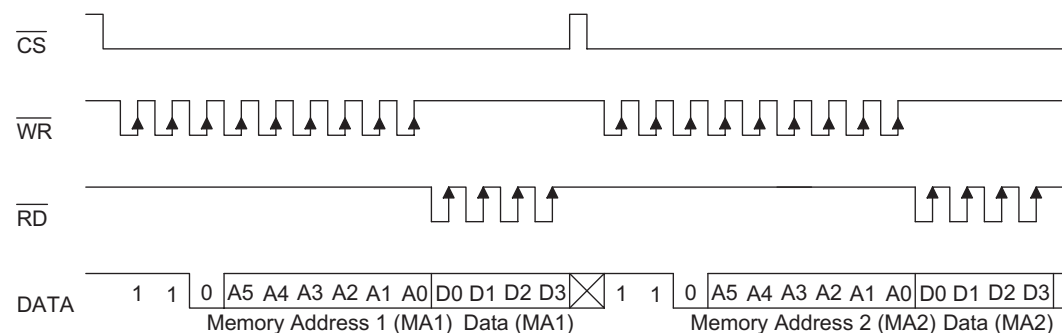
A 32768Hz crystal can be directly connected to the SHT32F21 via OSC1 and OSC0. In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table, which suggests the value of capacities. The table illustrates the suggestion value of capacities (C1, C2)

Crystal Error	Capacity Value
±10ppm	0~10p
10~20ppm	10~20p



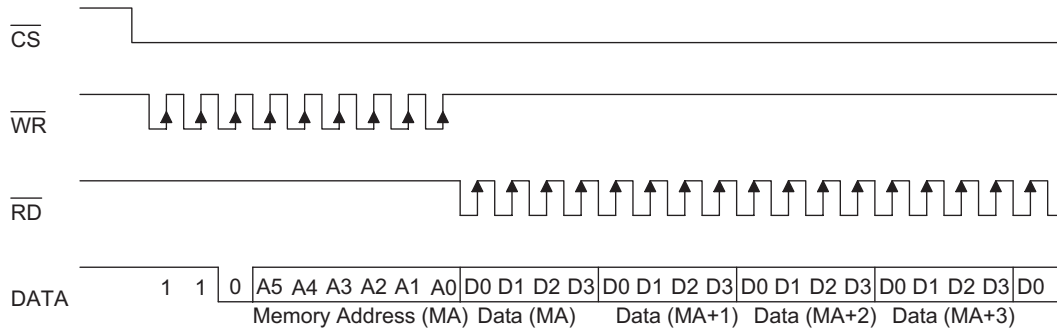
### Timing Diagrams

#### READ Mode (Command Code : 1 1 0)

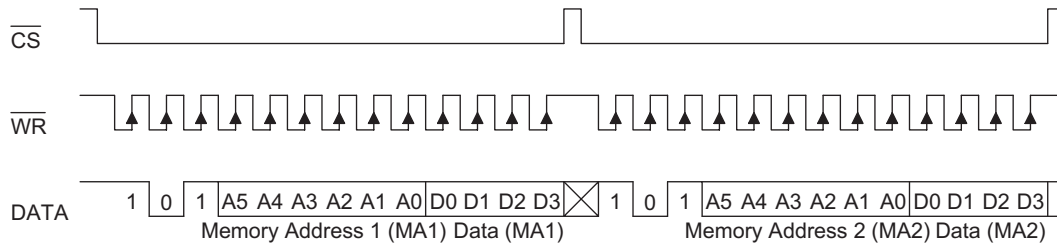


## RAM Mapping 32×4 LCD Controller

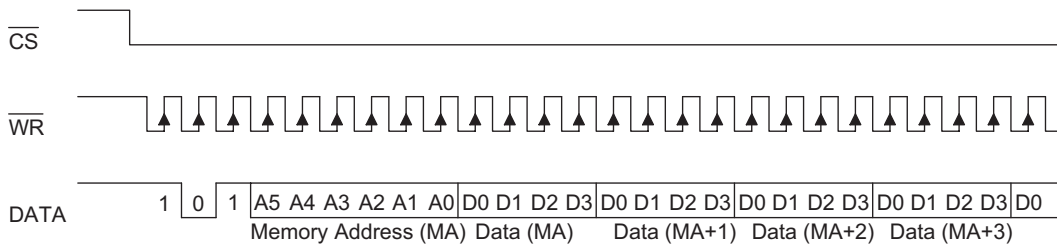
### READ Mode (Successive Address Reading)



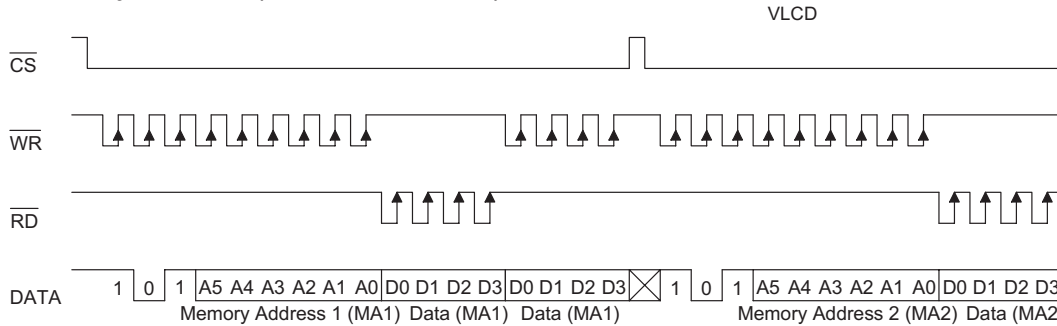
### WRITE Mode (Command Code : 1 0 1)



### WRITE Mode (Successive Address Writing)

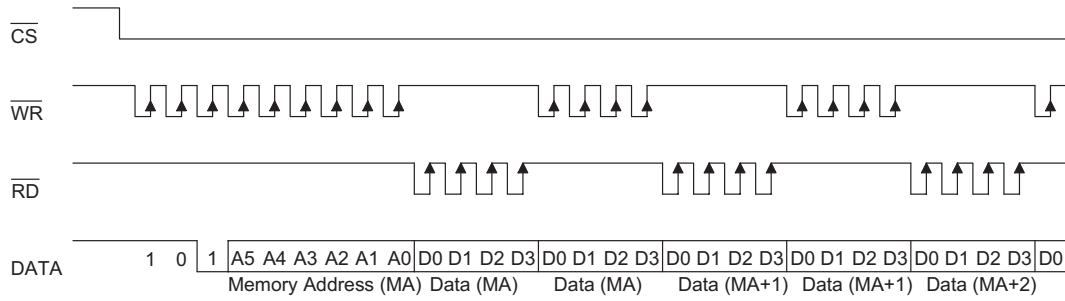


### Read-Modify-Write Mode (Command Code : 1 0 1)

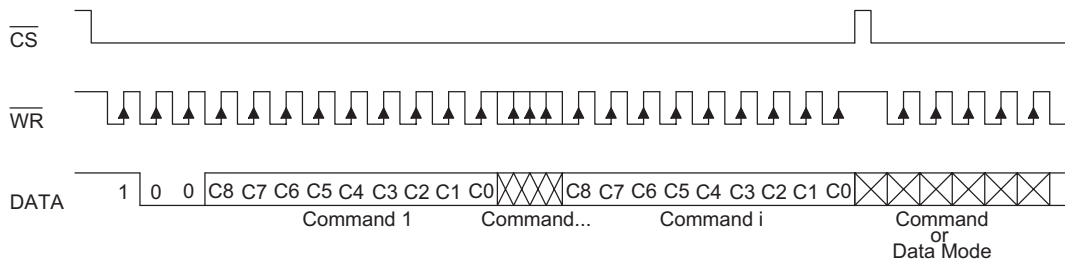


# RAM Mapping 32×4 LCD Controller

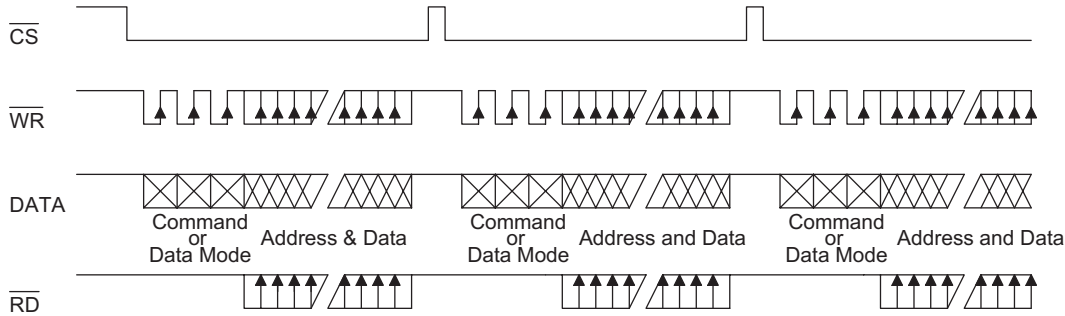
## Read-Modify-Write Mode (Successive Address Accessing)



## Command Mode (Command Code : 1 0 0)



## Mode (Data and Command Mode)

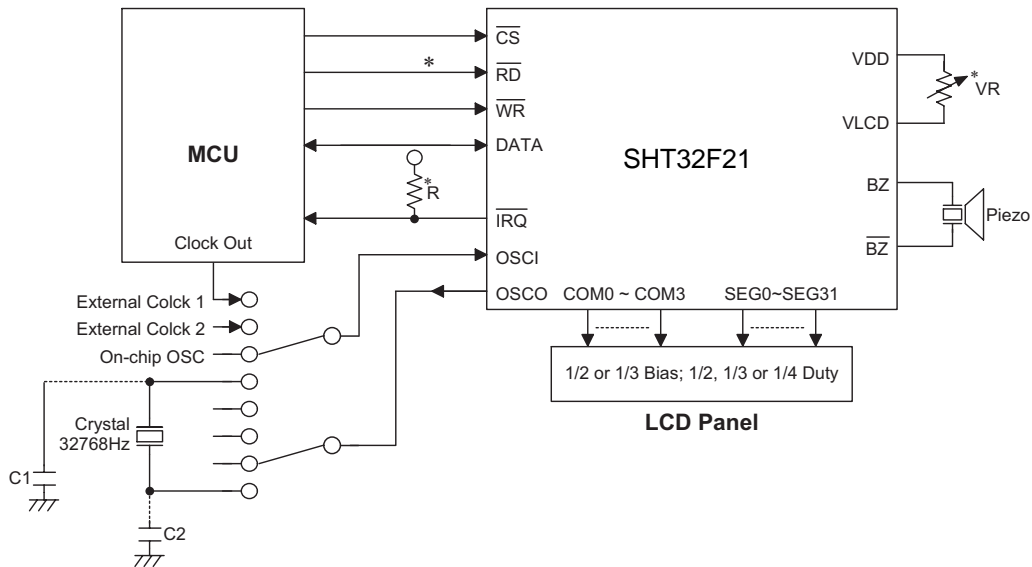


Note: It is recommended that the host controller should read in the data from the  $\overline{DATA}$  line between the rising edge of the  $\overline{RD}$  line and the falling edge of the next  $\overline{RD}$  line.

# RAM Mapping 32×4 LCD Controller

## Application Circuits

### Host Controller with an SHT32F21 Display System



Note: The connection of  $\overline{\text{IRQ}}$  and  $\overline{\text{RD}}$  pin can be selected depending on the requirement of the MCU.

The voltage applied to  $V_{\text{LCD}}$  pin must be lower than  $V_{\text{DD}}$ .

Adjust VR to fit LCD display, at  $V_{\text{DD}}=5\text{V}$ ,  $V_{\text{LCD}}=4\text{V}$ ,  $\text{VR}=15\text{k}\Omega\pm 20\%$ .

Adjust R (external pull-high resistance) to fit user's time base clock.

In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table, which suggests the value of capacities.

The table illustrates the suggestion value of capacities (C1,C2)

Crystal Error	Capacity Value
$\pm 10\text{ppm}$	0~10p
10~20ppm	10~20p

## Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	1 1 0	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	1 0 1	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	1 0 0	0000-0000-X	C	Turn off both system oscillator and LCD bias generator	Yes
SYS EN	1 0 0	0000-0001-X	C	Turn on system oscillator	
LCD OFF	1 0 0	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	1 0 0	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0	0000-0100-X	C	Disable time base output	
WDT DIS	1 0 0	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	1 0 0	0000-0110-X	C	Enable time base output	
WDT EN	1 0 0	0000-0111-X	C	Enable WDT time-out flag output	

## RAM Mapping 32×4 LCD Controller

Name	ID	Command Code	D/C	Function	Def.
TONE OFF	<b>1 0 0</b>	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	<b>1 0 0</b>	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	<b>1 0 0</b>	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	<b>1 0 0</b>	0000-111X-X	C	Clear the contents of WDT stage	
XTAL 32K	<b>1 0 0</b>	0001-01XX-X	C	System clock source, crystal oscillator	
RC 256K	<b>1 0 0</b>	0001-10XX-X	C	System clock source, on-chip RC oscillator	Yes
EXT 256K	<b>1 0 0</b>	0001-11XX-X	C	System clock source, external clock source	
BIAS 1/2	<b>1 0 0</b>	0010-abX0-X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1/3	<b>1 0 0</b>	0010-abX1-X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	<b>1 0 0</b>	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	<b>1 0 0</b>	011X-XXXX-X	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}} \text{ DIS}$	<b>1 0 0</b>	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}} \text{ EN}$	<b>1 0 0</b>	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	<b>1 0 0</b>	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	<b>1 0 0</b>	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	<b>1 0 0</b>	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	<b>1 0 0</b>	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	<b>1 0 0</b>	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	<b>1 0 0</b>	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	<b>1 0 0</b>	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	<b>1 0 0</b>	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	Yes
TEST	<b>1 0 0</b>	1110-0000-X	C	Test mode, user don't use.	
NORMAL	<b>1 0 0</b>	1110-0011-X	C	Normal mode	Yes

Note: X : Don't care

VLCD

A5~A0 : RAM addresses

D3~D0 : RAM data

D/C : Data/command mode

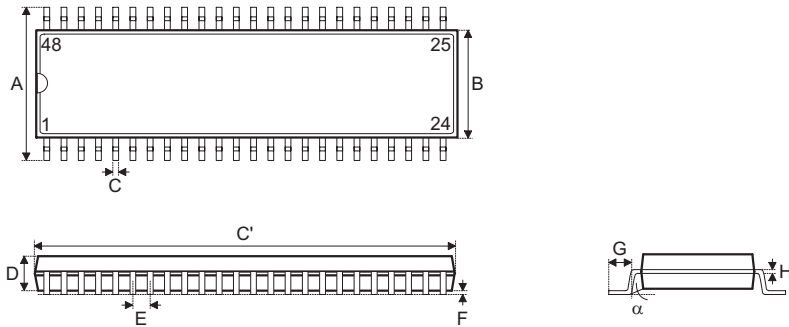
Def. : Power on reset default

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialize the SHT32F21 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the SHT32F21.

# RAM Mapping 32×4 LCD Controller

## Package Information

### 48-pin SSOP (300mil) Outline Dimensions

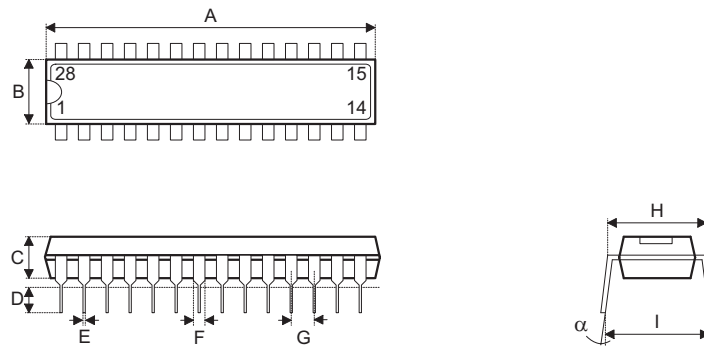


Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	395	—	420
B	291	—	299
C	8	—	12
C'	613	—	637
D	85	—	99
E	—	25	—
F	4	—	10
G	25	—	35
H	4	—	12
$\alpha$	0°	—	8°

VLCD

## RAM Mapping 32×4 LCD Controller

28-pin SKDIP (300mil) Outline Dimensions



Symbol	Dimensions in mil		
	Min.	Nom.	Max.
A	1375	—	1395
B	278	—	298
C	125	—	135
D	125	—	145
E	16	—	20
F	50	—	70
G	—	100	—
H	295	—	315
I	330	—	375
α	0°	—	15°

VLCD

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