DATA SHEET

TRUEVIEW™ 5725

Multimedia processor for HD PTV and LCD TV

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REVISION HISTORY

Revision	Description	Corresponding Page(s)
1.0	2011 version	
2.1	Add some details	
3.1	Add some details	
3.2	Add some details	

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INTRODUCTION

The TrueView5725 is a low pin count, low-cost advanced and highly integrated Digital and Analog Video Display Processor providing the key features needed to design HD-READY, Progressive scan or LCD Televisions

TrueView5725 accepts interlaced or progressive video input and graphic input such as NTSC/PAL, 1080i/720p, and SXGA, etc. in both analog and digital channels. It provides a high quality display output. It is capable of advanced de-interlacing, video enhancement, advanced 3D noise reduction, Y/C cross talk suppression and frame rate conversion. It also provides superior video output quality.

It integrates a complete triple 8-bit pipeline ADC with a clock-recovery and sync separation circuit to generate the sampling clock from HSYNC. In applications where the analog outputs are used the 24-bit digital pins can be inputs if the pins are not used for digital output.

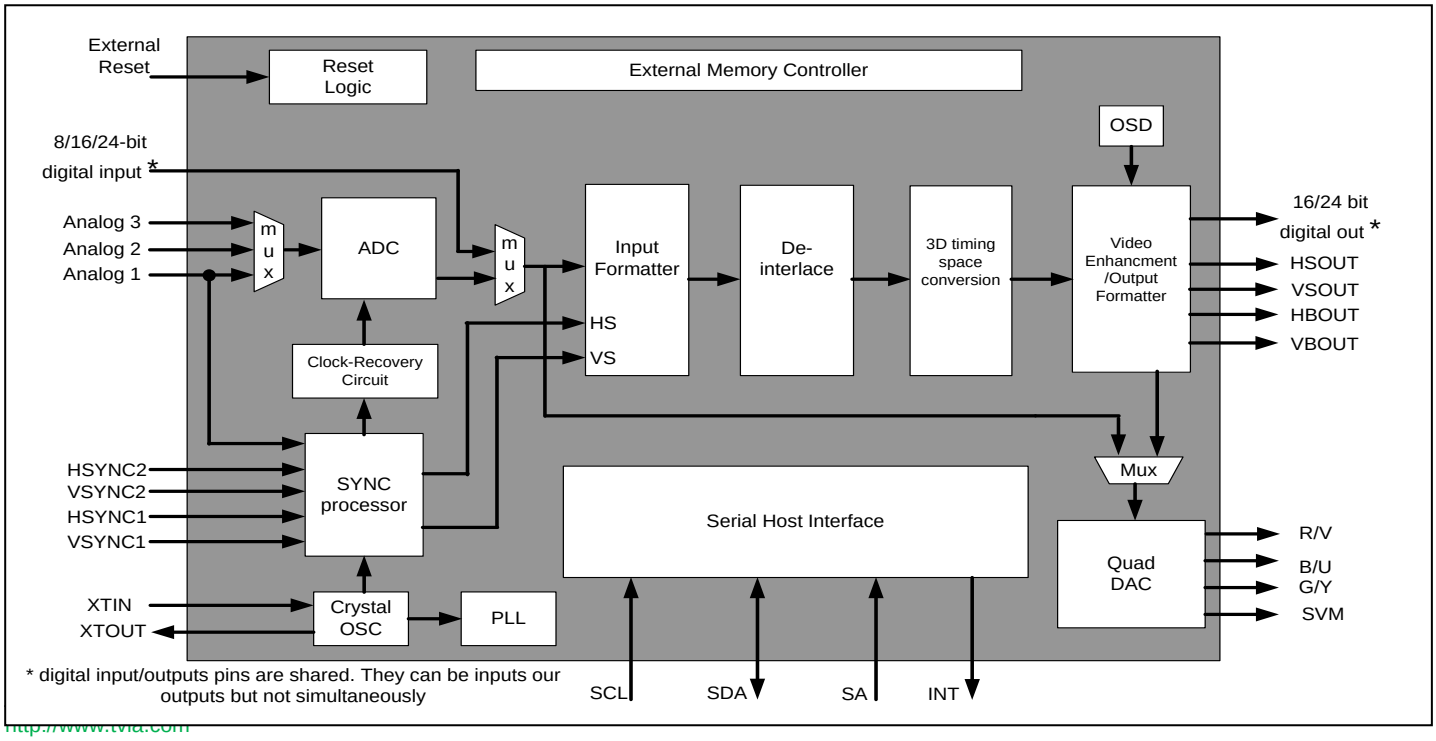
With the high quality video DACs, the video stream is displayed through its de-interlaced RGB/YPbPr outputs.

The I²C host interface enables OEMs to select from many different CPU's in order to meet their system and technical requirements.

OEMs can easily design a very low cost solution, while minimizing their software development time by leveraging on TrueView5725's level of integration and software support.

TrueView5725 provides 3D motion adaptive de-interlacing with diagonal edge detection. It performs high quality line doubling and high-accuracy non-linear motion estimation. It performs pixel based motion detection using two-field buffers. The Video De-interlacing Processor automatically detects noise level and can respond to different noise thresholds. It can also automatically detect input modes such as still images, 3:2 / 2:2 films and provide adaptive processing.

Figure 1: Block Diagram



FEATURES

- **Analog Input Formatter**
  - Max three channel analog inputs
  - RGB/YCbCr/YPbPr input
  - Analog input range: 0.5V – 1.0V (p-p)
  - Programmable gain/offset controls
  - DC or AC coupling inputs
  - Internal sync separator to support SOG/SOY
  - SXGA (1280x1024@75Hz) at 135MHz
  - HDTV up to 1080p
  - Macrovision input detection

- **Triple 8-bit ADC**
  - Maximum analog sampling rate up to 162MSPS

- **Clock-recovery Circuit**
  - Programmable phase adjustment cells
  - HSYNC frequency range is from 15KHz to 110KHz

- **Digital Input Formatter**
  - 24bit RGB/YUV input
  - 8/16bit YUV input
  - 8bit 656/601 input
  - NTSC/PAL input
  - 480p, 576p input
  - VGA/SVGA/XVGA input
  - 720p, 1080i, 1080p HD input
  - Support DVI interface

- **Output formatter**
  - 480p, 576p, 720p, 1080i, 1080p
  - Up to SXGA graphic output formats
  - 100/120 interlace double scan
  - 75Hz interlace single scan
  - 50-75Hz scan rate conversion
  - 15~80KHz horizontal frequency
  - 16bit YPbPr digital output with syncs
  - 24bit YPbPr/RGB digital output with syncs

- **De-interlace**
  - HD 1080i support
  - SD NTSC/PAL
  - Direct Edge Correction De-interlace
  - Motion Detection
  - Edge Detection
  - Mode Detection
  - Noise Detection
  - 3:2/2:2 pull-down detection

- **Memory Controller**
  - 2-8Mbyte memory support
  - 16/32bit data access

- **Video enhancement**
  - Black Level Expansion (BLE)
  - White Level Expansion (WLE)
  - Color Transition Improvement (DCTI)
  - Dynamic Range expansion
  - Brightness, Saturation, Contrast, HUE
  - Dynamic 2D Peaking
  - 2D coring
  - 3D noise reduction
  - Scan Velocity Modulation (SVM)
  - 2D Nonlinear scaling
  - Primary Color Enhancement
  - Skin Tone Enhancement
  - Blue Stretch

- **OSD**
  - Simple OSD generator to support component video inputs

- **Host Interface and I/O**
  - Two-wire I²C interface
  - GPIO

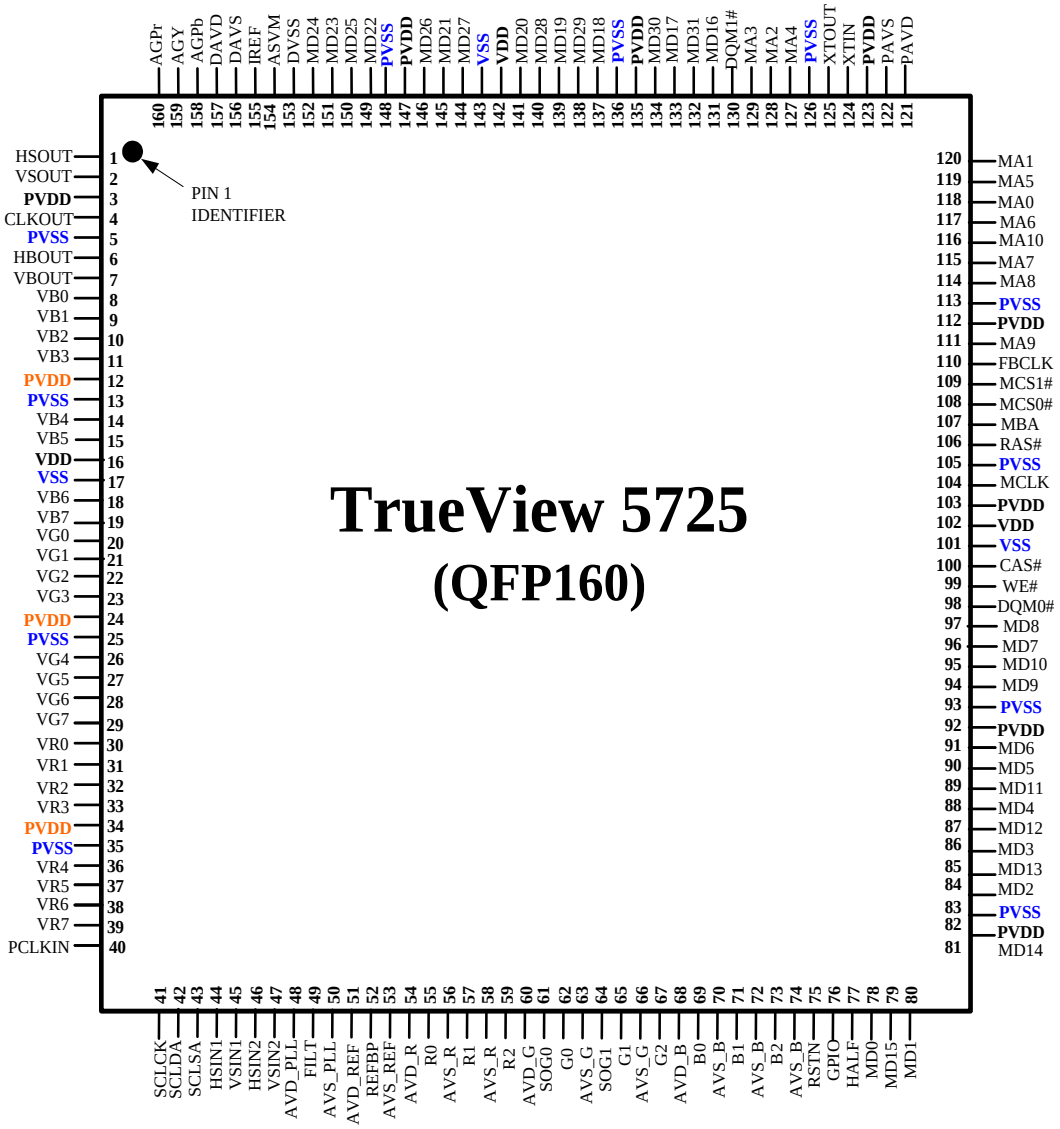
- **Quadruple 10bit DAC**

- **Package and Technology**
  - 160-pin QFP 28*28mm
  - 0.18 micron, 3.3V / 1.8V technology

Note: All packages are lead-free and RoHS compliant.

PINOUT DIAGRAM

PIN DIAGRAM FOR QFP160



PIN DESCRIPTION

Table 1: Digital Video Input Pins

Pin Name	QFP160 Pin #	Type	Pin Description
PCLKIN	40	IPD	Digital input video clock
HSIN1	44	I	Digital input video H-sync Shared with Analog input video H-sync1
VSIN1	45	I	Digital input video V-sync Shared with Analog input video V-sync1
VG [7:0]	29~26, 23~20	IOPD	Video Green Input data. • G data for 24bit RGB mode. • Y data for 4:4:4 mode • YUV data for 8bit 4:2:2 YUV mode. • Y/G data for 24bit input Shared with digital video output data
VB [7:0]	19~18, 15~14, 11~8	IOPD	Video Blue Input data. • B data for 24bit RGB mode. • U data for 4:4:4 YUV mode. • UV data for 16bit 4:2:2 YUV mode. • U/B data for 24bit input. • Y data for 16bit input. Shared with digital video output data
VR [7:0]	39~36, 33~30	IOPD	Video Red Input data. • R data for 24bit RGB mode. • V data for 4:4:4 mode. • Y data for 16bit 4:2:2 mode. • V/R data for 24bit input • U/V data for 16bit input Shared with digital video output data
CLKOUT	4	IO	Display enable input from DVI/HDMI decoder Shared with video clock output & GPIO bit 7
HSOUT	1	IO	Input H-sync for digital input mode Shared with H-sync output
VSOUT	2	IO	Input V-sync for digital input mode Shared with V-sync output
HALF	77	IOPD	Half tone input Shared with GPIO bit 1

Table 2: Digital Video Output Pins

Pin Name	QFP160 Pin #	Type	Pin Description
CLKOUT	4	IO	Digital video display output clock Shared with display enable input & GPIO bit 7
HSOUT	1	IO	Digital video display output H-sync Shared with H-sync input for digital input mode
VSOUT	2	IO	Digital video display output V-sync Shared with V-sync output for digital input mode

VBOUT	7	IO	Display enable output in LCD application Shared with GPIO bit 6 and V-blank output
VG [7:0]	29~26, 23~20	IOPD	• Y/G data for 24bit digital output. Shared with digital video input data
VB [7:0]	19~18, 15~14, 11~8	IOPD	• UV data for 16bit digital output. • R/V data for 24bit digital output. Shared with digital video input data
VR [7:0]	39~36, 33~30	IOPD	• Y data for 16bit digital output. • B/U data for 24bit digital output. Shared with digital video input data

Table 3: Analog Video input Pins

Pin Name	QFP160 Pin #	Type	Pin Description
HSIN1	44	I	Analog video input H-sync1 Shared with digital video input H-sync
VSIN1	45	I	Analog video input V-sync1 Shared with digital video input V-sync
HSIN2	46	I	Analog video input H-sync2
VSIN2	47	I	Analog video input V-sync2
SOG0	61	AI	Green input 0 for Sync-On-Green sync tip clamping
SOG1	64	AI	Green input 1 for Sync-On-Green sync tip clamping
R0	55	AI	Analog input for Red input channel 0
G0	62	AI	Analog input for Green input channel 0
B0	69	AI	Analog input for Blue input channel 0
R1	57	AI	Analog input for Red input channel 1
G1	65	AI	Analog input for Green input channel 1
B1	71	AI	Analog input for Blue input channel 1
R2	59	AI	Analog input for Red input channel 2
G2	67	AI	Analog input for Green input channel 2
B2	73	AI	Analog input for Blue input channel 2
REFBP	52	AI	Internal reference bypass
AVD_R	54	AP	Analog power (3.3V)
AVS_R	56, 58	AG	Analog ground
AVD_G	60	AP	Analog power (3.3V)
AVS_G	63, 66	AG	Analog ground
AVD_B	68	AP	Analog power (3.3V)
AVS_B	70, 72, 74	AG	Analog ground
AVD_REF	51	AP	Analog power (3.3V)
AVS_REF	53	AG	Analog ground
AVD_PLL	48	AP	Analog power (3.3V) for PLLAD
FILT	49	AI	Connection for External Filters components for PLLAD
AVS_PLL	50	AG	Analog ground for PLLAD

Table 4: Analog Video Output Interface Pins

Pin Name	QFP160 Pin #	Type	Pin Description
HSOUT	1	IO	Analog video display output H-sync Shared with H-sync input for digital input mode
VSOUT	2	IO	Analog video display output V-sync Shared with V-sync output for digital input mode
HBOUT	6	IO	Analog video display output H-Blank Shared with GPIO bit 5
VBOUT	7	IO	Analog video display output V-Blank Shared with GPIO bit 6 and DE output for digital video output
AGPb	158	AO	Analog Blue/Pb output
AGY	159	AO	Analog Green/Y output
AGPr	160	AO	Analog Red/Pr output
ASVM	154	AO	Analog SVM output
IREF	155	AI	Full-scale adjust resistor
DVSS	153	AG	Big current GND
DAVS	156	AG	Analog ground for DAC
DAVD	157	AP	Analog power for DAC

Table 5: Clock Generation Pins

Pin Name	QFP160 Pin #	Type	Pin Description
XTOUT	125	O	External crystal output.
XTIN	124	I	External crystal input.
PAVD	121	AP	Analog power (3.3V) for PLL648
PAVS	122	AG	Analog ground for PLL648

Table 6: System Interface Pins

Pin Name	QFP160 Pin #	Type	Pin Description
SCLSA	43	IOPU	Serial bus slave address selection, Shared with GPIO bit 2
SCLCK	41	I	Serial bus clock
SCLDA	42	IO	Serial bus data
RSTN	75	I	External asynchronous reset, low active
GPIO	76	IOPD	GPIO bit 0 Shared with Interrupt Output, low active

Table 7: SDRAM Interface Pins

Pin Name	QFP160 Pin #	Type	Pin Description
MD31	132	IOPD	**Memory Data Bus [31:0]**
MD30	134	IOPD	
MD29	138	IOPD	
MD28	140	IOPD	
MD27	144	IOPD	
MD26	146	IOPD	
MD25	150	IOPD	
MD24	152	IOPD	
MD23	151	IOPD	
MD22	149	IOPD	
MD21	145	IOPD	
MD20	141	IOPD	
MD19	139	IOPD	
MD18	137	IOPD	
MD17	133	IOPD	
MD16	131	IOPD	
MD15	79	IOPD	
MD14	81	IOPD	
MD13	85	IOPD	
MD12	87	IOPD	
MD11	89	IOPD	
MD10	95	IOPD	
MD9	94	IOPD	
MD8	97	IOPD	
MD7	96	IOPD	
MD6	91	IOPD	
MD5	90	IOPD	
MD4	88	IOPD	
MD3	86	IOPD	
MD2	84	IOPD	
MD1	80	IOPD	
MD0	78	IOPD	
DQM0#	98	O	Memory data qualify signal 0
DQM1#	130	O	Memory data qualify signal 1
MCLK	104	O	SDRAM clock
WE#	99	O	Write enable control for SDRAM
RAS#	106	O	Row address strobe
CAS#	100	O	Column address strobe
FBCLK	110	IOPD	Feed back clock for SDRAM Chip Selection 2 for 6MByte external memory
MBA	107	IOPD	SDRAM bank select Shared with GPIO bit 3

Pin Name	QFP160 Pin #	Type	Pin Description
MCS1#	109	IOPD	Memory chip Selection 1, And shared with GPIO bit 4.
MCS0#	108	IOPD	Memory chip Selection 0
MA10	116	IOPD	**Memory address bus [10:0]**
MA9	111	IOPD	
MA8	114	IOPD	
MA7	115	IOPD	
MA6	117	IOPD	
MA5	119	IOPD	
MA4	127	IOPD	
MA3	129	IOPD	
MA2	128	IOPD	
MA1	120	IOPD	
MA0	118	IOPD	

Table 8: Digital Power and Ground Pins

Pin Name	QFP160 Pin #	Type	Pin Description
VSS	17,101,143	DG	Core Power GND
VDD	16,102,142	DP	1.8V Core Power
PVDD	3, 12, 24, 34, 82, 92, 103, 112, 123, 135, 147,	DP	**3.3V I/O Power**
PVSS	5, 13, 25, 35, 83, 93, 105, 113, 126, 136, 148	DG	I/O GND

Pin types include the following:

- I Digital Input
- IPD Digital Input with pull-down
- O Digital Output
- OPD Digital Output with pull-down
- IO Digital Bi-directional (input/output)
- IOPU Digital Bi-directional (input/output) with pull-up
- IOPD Digital Bi-directional (input/output) with pull-down
- AI Analog Input
- AO Analog Output
- DP Digital Power
- DG Digital Ground
- AP Analog Power
- AG Analog Ground

Table 9: Numerical Pin List

Pin Name	QFP160 Pin #	Pin Name	QFP160 Pin #	Pin Name	QFP160 Pin #	Pin Name	QFP160 Pin #
HSOUT	1	SCLCK	41	MD14	81	PAVD	121
VSOUT	2	SCLDA	42	PVDD	82	PAVS	122
PVDD	3	SCLSA	43			PVDD	123
PVDD		HSIN1	44	PVSS	83		
CLKOUT	4	VSIN1	45	MD2	84	XTIN	124
PVSS	5	HSIN2	46	MD13	85	XTOUT	125
PVSS		VSIN2	47	MD3	86	PVSS	126
HBOUT	6	AVD_PLL	48	MD12	87	PVSS	
VBOUT	7	AVD_PLL		MD4	88	MA4	127
VB0	8	FILT	49	MD11	89	MA2	128
VB1	9	AVS_PLL	50	MD5	90	MA3	129
VB2	10	AVD_REF	51	MD6	91	DQM1	130
VB3	11	REFBP	52	PVDD	92	MD16	131
PVDD	12	AVS_REF	53	PVSS	93	MD31	132
PVSS	13	AVD_R	54	MD9	94	MD17	133
VB4	14	AVD_R		MD10	95	MD30	134
VB5	15	R0	55	MD7	96	PVDD	135
VDD	16	AVS_R	56	MD8	97	PVSS	136
VDD		R1	57	DQM0	98	MD18	137
VSS	17	AVS_R	58	WE#	99	MD29	138
VB6	18	R2	59	CAS#	100	MD19	139
VB7	19	AVD_G	60	VSS	101	MD28	140
VG0	20	AVD_G		VDD	102	MD20	141
VG1	21	SOG0	61	VDD		VDD	142
VG2	22	G0	62	PVDD	103	VDD	
VG3	23	AVS_G	63	PVDD		VSS	143
PVDD	24	SOG1	64	MCLK	104	VSS	
PVSS	25	G1	65	PVSS	105	MD27	144
VG4	26	AVS_G	66	PVSS		MD21	145
VG5	27	G2	67	RAS#	106	MD26	146
VG6	28	AVD_B	68	MBA	107	PVDD	147
VG7	29	AVD_B		MCS0#	108	PVSS	148
VR0	30	B0	69	MCS1#	109	MD22	149
VR1	31	AVS_B	70	FBCLK	110	MD25	150
VR2	32	B1	71	MA9	111	MD23	151
VR3	33	AVS_B	72	PVDD	112	MD24	152
PVDD	34	B2	73	PVSS	113	DVSS	153
PVDD		AVS_B	74	MA8	114	ASVM	154
PVSS	35	RSTN	75	MA7	115	IREF	155
VR4	36	GPIO	76	MA10	116	DAVS	156
VR5	37	HALF	77	MA6	117	DAVD	157
VR6	38	MD0	78	MA0	118	AGPb	158
VR7	39	MD15	79	MA5	119	AGY	159
PCLKIN	40	MD1	80	MA1	120	AGPr	160

FUNCTIONAL DESCRIPTION

The TrueView 5725 TV Display Processor consists of a number of functional blocks which are described below.

ADC

The ADC can accommodate input signals with inputs ranging from 0.5V to 1.0V full scale. The full-scale range is set in three 8-bit registers (Red Gain, Green Gain, and Blue Gain).
The ADC offset control shifts the input source a DC level, there are three 7-bit registers (Red Offset, Green Offset, Blue Offset) available to independently control each channel, The offset controls provide a ± 63 LSB adjustment range. If the input range is 1.0V, the adjustable range is ±0.25V. Every step is 4mV (0.25 / 63 = 0.004V). If the input range is 0.5V, the adjustable range is ±0.125V. Every step is 2mV (0.125 / 63 = 0.002V).
The ADC has three input data channels, two SOG input channels and two separate H/V-sync input channels. It also generates an over-sampling clock from H-sync with a frequency range from lower than 10MHz up to 162Mhz.

INPUT FORMATTER

The Input Formatter accepts video data in several formats.

- 24-bit YCbCr or RGB
- 4:4:4 or 4:2:2
- 8 bit ITU-R BT.656
- 8 or 16 or 24 bit ITU-R BT.601
- NTSC or PAL
- 24 bit VGA (800*525@60Hz), SVGA, XGA and SXGA
- 1080i, 720p, 1080p, HD

The True View 5725 can automatically detect all supported monitor and TV modes including NTSC, PAL, VGA, SVGA, XGA, SXGA and HD modes and their supported refresh rate.

DE-INTERLACER

The TrueView5725 Motion Adaptive De-interlacer automatically determines the type of incoming video content such as film, static interlaced or moving interlaced video. Different algorithms are applied for each content type. The de-interlacer produces a progressive scan video output. Noise which otherwise would be seen as motion can be removed during motion processing. It also uses an edge detection algorithm that enables the smoothing of jagged edges that could occur in the de-interlacing process. Several different detection angles can be programmed.

FILM MODE

The De-interlace Processor can detect video that has originated from film and detects 3:2 or 2:2 pull down. If film originated video is detected the two fields from the original frame are combined into one progressive frame.

Thirty frames per second interlaced video can be output as 60 or 72Hz progressive frames.

Twenty-five frames per second interlaced video can be output as 50 or 75Hz progressive frames, or 100Hz-interlaced fields.

The de-interlacer continuously monitors the incoming video to detect any changes to the pull-down sequence. If a change is detected the deinterlacer quickly adapts its de-interlacing algorithm to compensate.

3D TIME – SPACE CONVERTER

The 3D Time – Space converter is used to alter the size of the picture depending on the output resolution. It contains an Up-Down scaler and Rate converter.

VIDEO PROCESSING

The Video Enhancer is a high-quality programmable processor that brings out details and color in the video.

Output Formatter

The Output formatter formats the output to give the required levels for RGB or YPbPr. It contains a 2X interpolator to increase sharpness that results from a smaller aperture.

Transient Improvement

Digital Chroma Transient improvement (DCTI) improves video by replacing slower edges of the video with edges that have steeper rise and fall times. DCTI turns sloped or sinusoidal waveforms into rectangular or square waveforms with the same duty cycles and peak-to-peak amplitude. It improves the color transitions of vertical objects and reduces color smearing introduced by a video decoder.

Black & white Level Expansion

The black and white-level expander enhances the contrast of the picture. The luminance signal is modified with an adjustable, non-linear function. Dark areas of the picture are made blacker, while bright areas of the picture are made whiter.

2D Peaking

Especially if the input signals are decoded composite signals and a notch filter has been used for luminance/color separation, it is necessary to improve the luminance/color frequency characteristics. The TrueView5725 2D peaking process uses edge enhancement to improve the Y and C sharpness in the vertical and horizontal directions. For Y, there is 2D peaking and for UV, there is only vertical peaking.

Skin tone correction

Skin tone correction is used to alter skin color to make it look more natural.

Non-linear saturation

Non-linear saturation is used to enhance the saturation of some colors without affecting other colors. Both the Y and UV parameters of the range of colors to be enhanced are programmable.

Brightness and Contrast

Brightness and contrast can be programmed by adjusting the offset and gain of the video signal. Contrast is adjusted by multiplying the luminance by a constant. Brightness is adjusted by adding or subtracting a constant, from the luminance value.

Saturation

Saturation can be changed by changing the UV gain of the color signal

Hue

The Hue of the color can be changed by rotating the UV vectors in either direction.

Background Noise Reduction

Background noise reduction is a process that uses a digital filtering algorithm on the digital image data to reduce the amount of random noise such as RF noise or comb filter artifacts in composite video sources etc. It is 3D motion adaptive and pixel based

Scan Velocity Modulation

The Scan Velocity Modulation (SVM) output is used to modulate the horizontal CRT scan timing. It has the effect of sharpening the transitions from dark to light and light to dark which results in a clearer sharper picture.

ANALOG AND DIGITAL OUTPUT

The Analog Display Port generates the analog RGB or YPbPr with triple Digital-to-Analog Converters (DACs). The DAC's have 10-bit quality. The analog RGB or YPbPr output is generated in synchronization with H and V timing signals. The 16-bit YCbCr digital output is ITU-R BT.601 compatible with a 1 X clock. The output comes from the 3D time-space converter block and is in 4:2:2 format.

MEMORY CONTROLLER

The internal Memory Controller supports the addressing and control of up to 8MB of external SDRAM. The external SDRAM memory buffer is used to store video fields and motion data. The Memory Controller also supports frame rate up-conversion with different input and output refresh rates.

PLL AND OSCILLATOR

The TrueView 5725 integrates a PLL to generate the MCLK to the Memory interface and the VCLK to the display. Only an external crystal is required to be connected between the XTIN and XTOUT pins. On power-up, the PLL is initialized to provide a 108 MHz MCLK and a 27 MHz VCLK when a 27MHz reference is used. Alternatively, the MCLK and VCLK can be driven directly by external clocks.

HOST BUS INTERFACE

Access to the TrueView 5725 registers is provided by an I²C 2-wire serial bus interface. The Interface

supports standard and fast modes, up to 400kbits/S. Only slave mode is supported in the TrueView 5725 TV Display Processor.

The slave address is hardware selectable.

Table 10: I²C Slave Addresses

TrueView 5725 I²C slave addresses	
Read	Write
2F	2E
AF	AE

OSD

The TrueView 5725 OSD engine is a simple eight icon, hardware graphic engine. It consists of eight 13x13 hard-wired OSD ROM locations containing the most common TV OSD symbols. Brightness, contrast, hue, sound, up/down adjustment, left/right adjustment, horizontal size adjustment, and vertical size adjustment.

Figure 2: OSD Icons

One of eight foreground and background colors can be selected and they can be zoomed in the horizontal or vertical direction up to eight times horizontally and four times vertically.

CLOCK RECOVERY CIRCUITS

The clock recovery circuit generates the ADC sampling clock and its over-sampling clock up to 162Mhz.The hsync signal can also be recovered from the PLL even when the input clock reference is a composite sync signal. This is achieved by sending a COAST high signal to the PLL to disable the PLL from tracking the input reference and to maintain the PLL output clock frequency if the input reference is not a regular period hsync signal. FS, KS and ICP registers are used to optimize the PLL performance for each specific video format. The CKOS register is used to control the over-sampling ratio. The following table gives the possible over-sampling cases. The over sampling ratio is determined by the relationship of the KS and CKOS register values.

Table 11: Over sampling ratio

KS	CKOS	OSR
00	00	1
01	00	2
	01	1
10	00	4
	01	2
	10	1

APPLICATION NOTES

ADC PIN CONNECTION

The analog RGB signals are connected to the TrueView5725 as shown below:

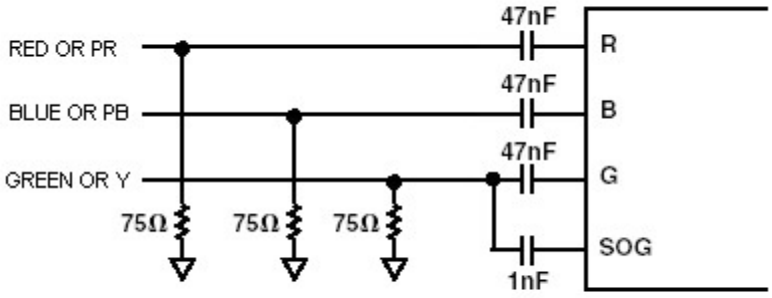


Figure 3: Example ADC Signal Connection

CRYSTAL PIN

1. EXTERNAL

XTIN and XTOUT are the input and output, respectively, of an inverting amplifier, which can be configured for use as an on-chip oscillator, as shown below. A 27 MHz crystal is preferred. In addition to an external crystal, the oscillator requires two external capacitors and an external feedback resistor.

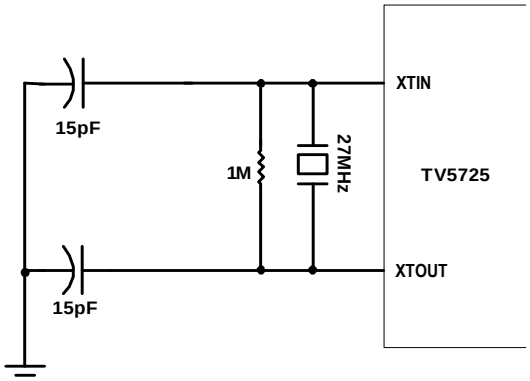


Figure 4: Crystal Connection Diagram

To drive the device from an external clock source, XTIN should be driven, while XTOUT floats, as shown below.

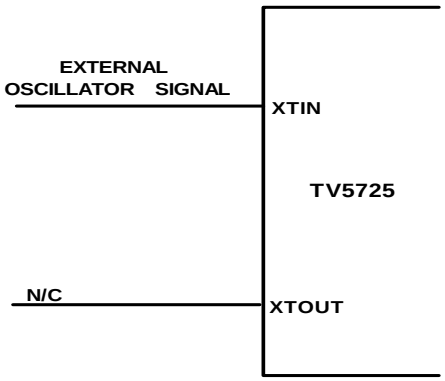


Figure 5: External Clock Drive Configuration

2. INTERNAL

C[2:0] are register bits, for changing the clock driver drive capability. The default value is 0 as shown below. SMT_EN_O is the register bit to select between a TTL or Schmitt trigger input buffer.

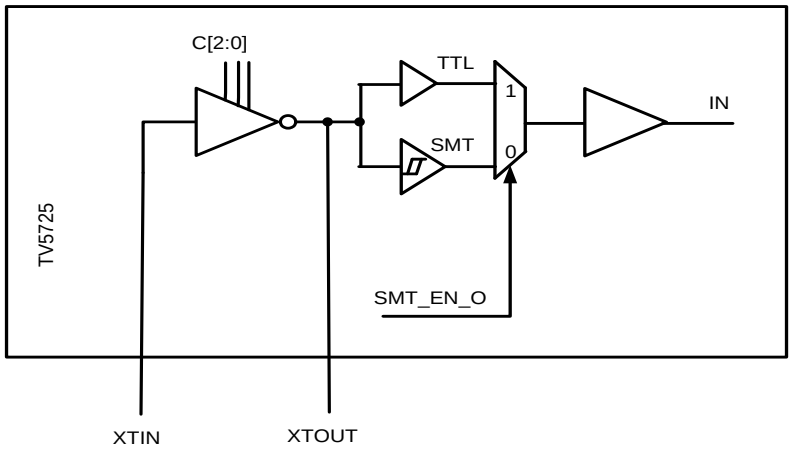


Figure 6: Internal Driver Configuration

VIDEO PORT USAGE

The TrueView 5725 has both analog and digital video input ports.

For analog input port:

- Three ADC input channels 0, 1, 2
- Two separate sync h/v or composite sync for ADC channels 0, 1, 2
- Two SOG inputs for ADC input channels 0, 1

For analog output port:

- One set of RGBS, H/V-sync, H/V-blank outputs
- It can output sync-on-Y YPbPr or sync-on-green RGB signal

For digital input port:

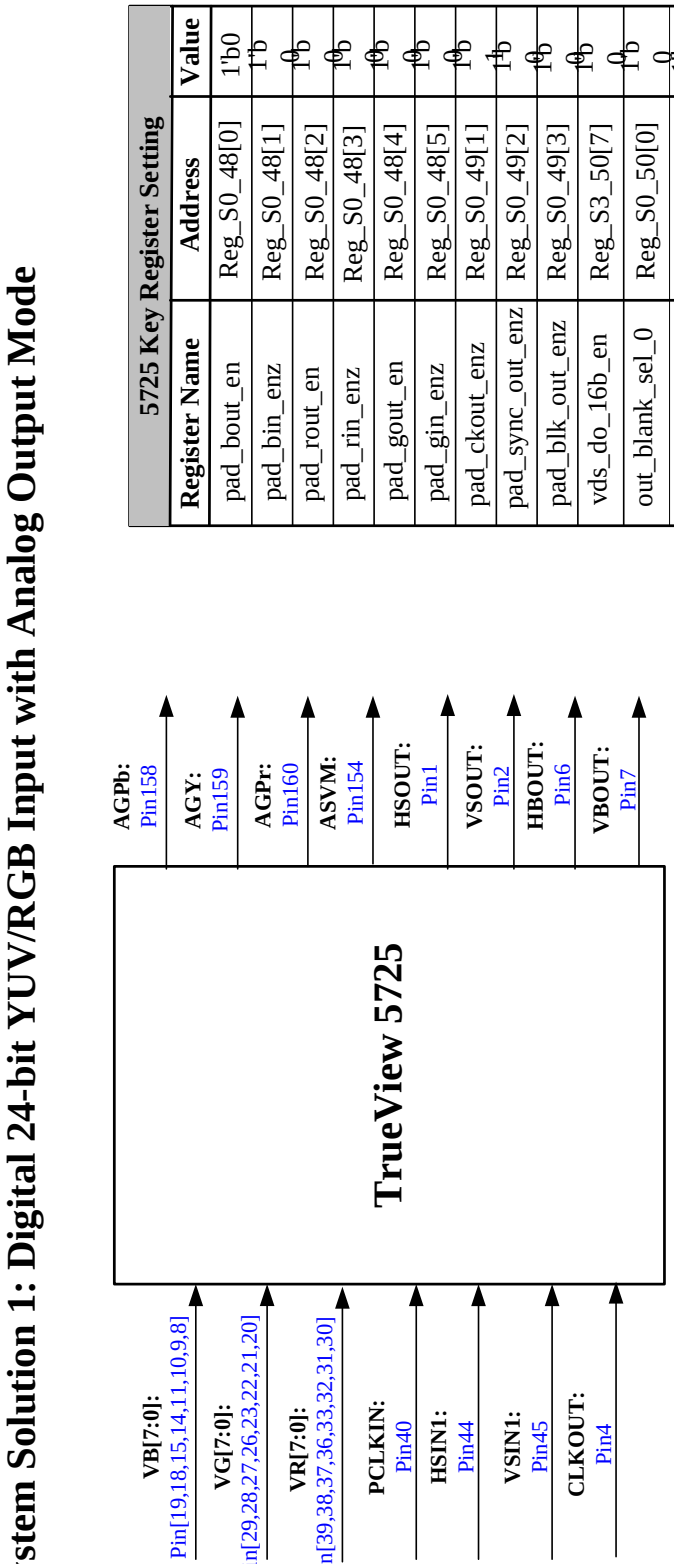
- One digital 24-bit input port
- 8-bit 601/656 YUV, 16-bit YUV, 24-bit YUV/RGB input
- De-in (display enable input) signal

For digital output port:

- Shared with 24-bit digital input port
- 16-bit YUV, 24-bit YUV/RGB.
- De-out (display enable output) signal
- H/V-sync and pixel clock
- H/V Blank <----------Note: H/V blank could be used for letter-box mode and pillar-box mode

The following pages show the port usage and corresponding register programming:

Figure 7: Digital 24-bit YUV/RGB Input with Analog Output Mode



Input Pin	Description	Output Pin	Description
VB[7:0]	Digital Blue/U data input	AGPb	Analog Blue/Pb output
VG[7:0]	Digital Green/Y data input	AGY	Analog Green/Y output
VR[7:0]	Digital Red/V data input	AGPr	Analog Red/Pr output
PCLKIN	Pixel clock input	ASVM	Analog SVM output
HSIN1	Video H-sync input	HSOUT	Video H-sync output
VSIN1	Video V-sync input	VSOUT	Video V-sync output
CLKOUT	DE input from DVI/HDMI	HBOUT	Video H-blank output
		VBOUT	Video V-blank output

5725 Key Register Setting		
Register Name	**Address**	**Value**
pad_bout_en	Reg_S0_48[0]	1'b0
pad_bin_enz	Reg_S0_48[1]	1'b0
pad_rout_en	Reg_S0_48[2]	1'b0
pad_rin_enz	Reg_S0_48[3]	1'b0
pad_gout_en	Reg_S0_48[4]	1'b0
pad_gin_enz	Reg_S0_48[5]	1'b0
pad_ckout_enz	Reg_S0_49[1]	1'b0
pad_sync_out_enz	Reg_S0_49[2]	1'b1
pad_blk_out_enz	Reg_S0_49[3]	1'b0
vds_do_16b_en	Reg_S3_50[7]	1'b0
out_blank_sel_0	Reg_S0_50[0]	1'b0
if_sel_adc_sync	Reg_S1_28[2]	1'b0
if_sel_656	Reg_S1_00[3]	1'b0
if_sel16bit	Reg_S1_00[4]	X
if_sel24bit	Reg_S1_01[7]	1'b1

Note: "X" means either "0" or "1" is OK.

System Solution 2: Digital 16-bit YUV 4:2:2 Input with Analog Output Mode

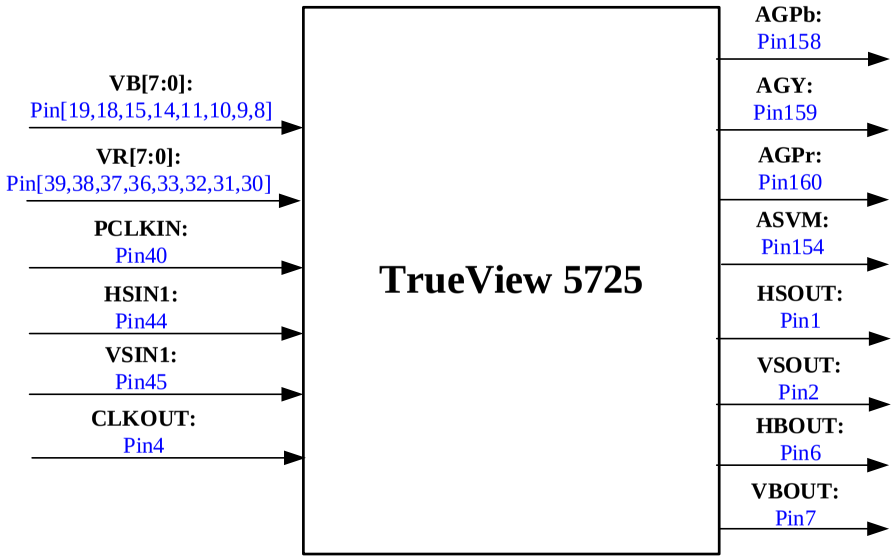


Figure 8: Digital 16-bit YUV 4:2:2 Input with Analog Output Mode

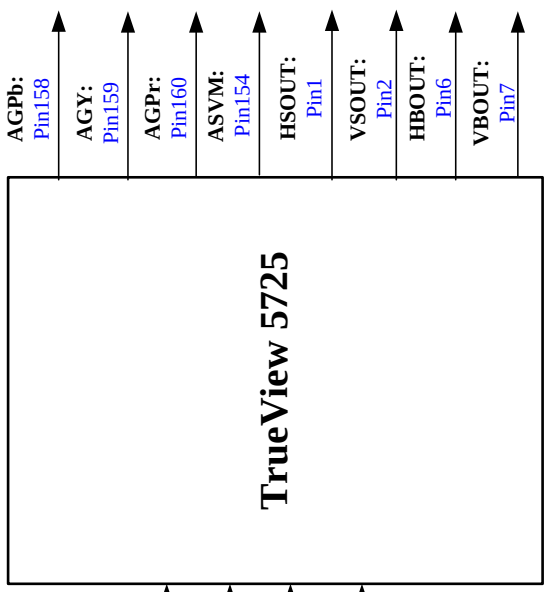
5725 Key Register Setting		
Register Name	**Address**	**Value**
pad_bout_en	Reg_S0_48[0]	1'b0
pad_bin_enz	Reg_S0_48[1]	1'b0
pad_rout_en	Reg_S0_48[2]	1'b0
pad_rin_enz	Reg_S0_48[3]	1'b0
pad_gout_en	Reg_S0_48[4]	X
pad_gin_enz	Reg_S0_48[5]	X
pad_ckout_enz	Reg_S0_49[1]	1'b1
pad_sync_out_enz	Reg_S0_49[2]	1'b0
pad_blk_out_enz	Reg_S0_49[3]	1'b0
vds_do_16b_en	Reg_S3_50[7]	1'b0
out_blank_sel_0	Reg_S0_50[0]	1'b0
if_sel_adc_sync	Reg_S1_28[2]	1'b0
if_sel_656	Reg_S1_00[3]	1'b0
if_sel16bit	Reg_S1_00[4]	1'b1
if_sel24bit	Reg_S1_01[7]	1'b0

Note: "X" means either "0" or "1" is OK.

Input Pin	Description	Output Pin	Description
VB[7:0]	Digital UV data input	AGPb	Analog Blue/Pb output
VR[7:0]	Digital Y data input	AGY	Analog Green/Y output
PCLKIN	Pixel clock input	AGPr	Analog Red/Pr output
HSIN1	Video H-sync input	ASVM	Analog SVM output
VSIN1	Video V-sync input	HSOUT	Video H-sync output
CLKOUT	DE input from DVI/HDMI	VSOUT	Video V-sync output
		HBOUT	Video H-blank output
		VBOUT	Video V-blank output

Figure 9: Digital 8-bit 601/656 4:2:2 YUV Input with Analog Output Mode

System Solution 3: Digital 8-bit 601/656 4:2:2 YUV Input with Analog Output Mode

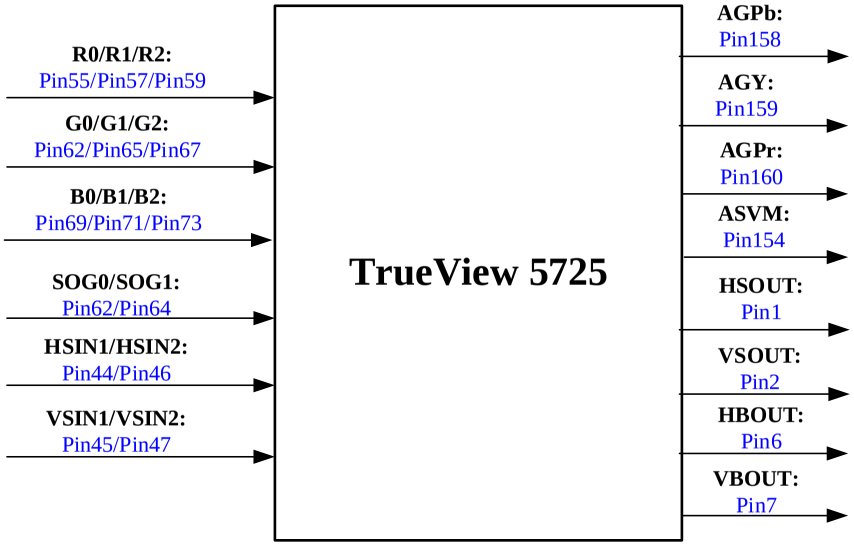


5725 Key Register Setting		
Register Name	**Address**	**Value**
pad_bout_en	Reg_S0_48[0]	X
pad_bin_enz	Reg_S0_48[1]	X
pad_rout_en	Reg_S0_48[2]	X
pad_rin_enz	Reg_S0_48[3]	X
pad_gout_en	Reg_S0_48[4]	1'b 0
pad_gin_enz	Reg_S0_48[5]	1'b 0
pad_ckout_enz	Reg_S0_49[1]	X
pad_sync_out_enz	Reg_S0_49[2]	1'b 0
pad_blk_out_enz	Reg_S0_49[3]	1'b 0
vds_do_16b_en	Reg_S3_50[7]	1'b 0
out_blank_sel_0	Reg_S0_50[0]	1'b 0
if_sel_adc_sync	Reg_S1_28[2]	1'b 0
if_sel_656	Reg_S1_00[3]	Note*
if_sel16bit	Reg_S1_00[4]	1'b0
if_sel24bit	Reg_S1_01[7]	1'b 0

Note: "X" means either "0" or "1" is OK.
Note* : if 656 input , set it to 1;
if 601 input , set it to 0.

Input Pin	Description	Output Pin	Description
VG[7:0]	Digital YUV data input	AGPb	Analog Blue/Pb output
PCLKIN	Pixel clock input	AGY	Analog Green/Y output
HSIN1	Video H-sync input	AGPr	Analog Red/Pr output
VSIN1	Video V-sync input	ASVM	Analog SVM output
		HSOUT	Video H-sync output
		VSOUT	Video V-sync output
		HBOUT	Video H-blank output
		VBOUT	Video V-blank output

System Solution 4: Analog YUV/RGB Input with Analog Output Mode



Input Pin	Description	Output Pin	Description
R0/R1/R2	Analog R/V input of CHN0/1/2	AGPb	Analog Blue/Pb output
G0/G1/G2	Analog G/Y input of CHN0/1/2	AGY	Analog Green/Y output
B0/B1/B2	Analog B/U input of CHN0/1/2	AGPr	Analog Red/Pr output
SOG0/SOG1	Analog SOG/Y input of CHN0/1	ASVM	Analog SVM output
HSIN1/HSIN2	Video H-sync input 1/2*	HSOUT	Video H-sync output
VSIN1/VSIN2	Video V-sync input 1/2*	VSOUT	Video V-sync output
		HBOUT	Video H-blank output
		VBOUT	Video V-blank output

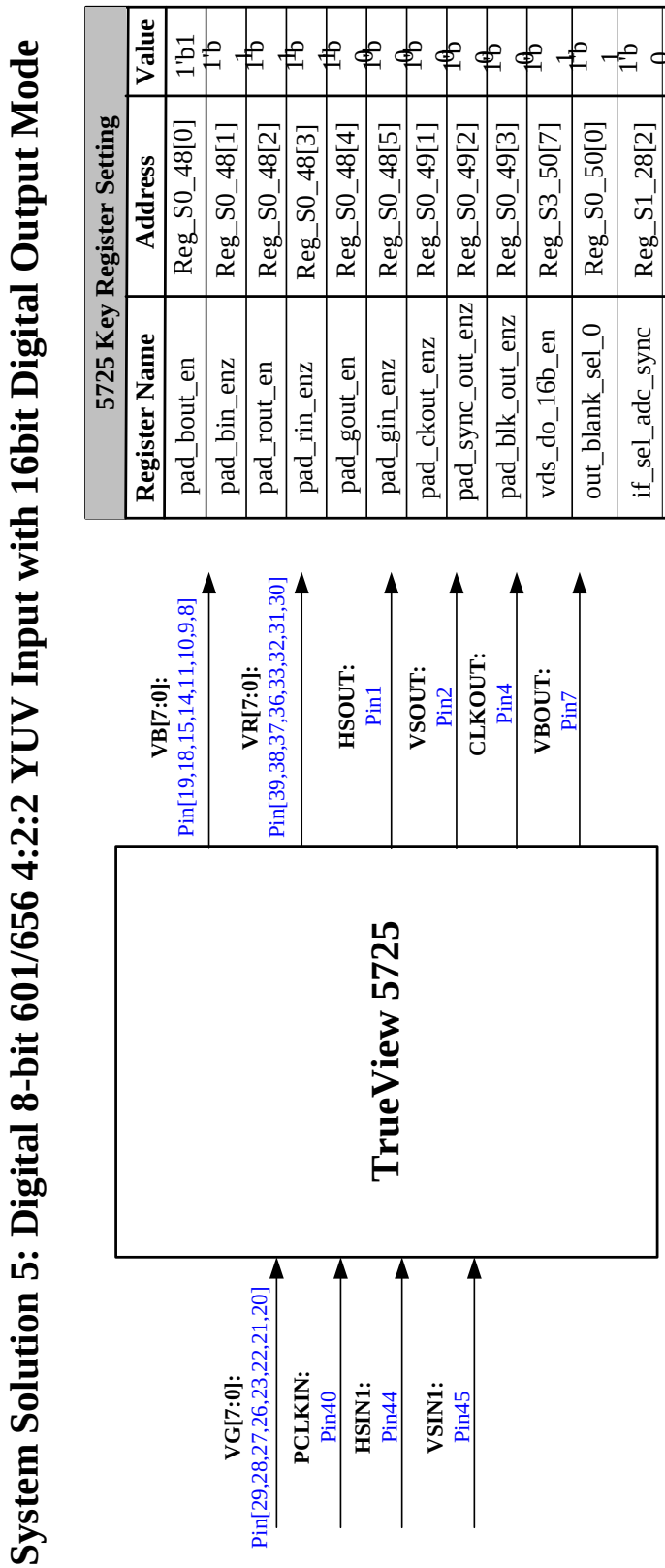
Note*: HSIN1/VSIN1 and HSIN2/VSIN2 could be programmed for analog channel 0/1/2

5725 Key Register Setting		
Register Name	**Address**	**Value**
pad_bout_en	Reg_S0_48[0]	X
pad_bin_enz	Reg_S0_48[1]	X
pad_rout_en	Reg_S0_48[2]	X
pad_rin_enz	Reg_S0_48[3]	X
pad_gout_en	Reg_S0_48[4]	X
pad_gin_enz	Reg_S0_48[5]	X
pad_ckout_enz	Reg_S0_49[1]	X
pad_sync_out_enz	Reg_S0_49[2]	1'b0
pad_blk_out_enz	Reg_S0_49[3]	1'b0
vds_do_16b_en	Reg_S3_50[7]	1'b0
out_blank_sel_0	Reg_S0_50[0]	1'b0
if_sel_adc_sync	Reg_S1_28[2]	1'b1
if_sel_656	Reg_S1_00[3]	1'b0
if_sel16bit	Reg_S1_00[4]	X
if_sel24bit	Reg_S1_01[7]	1'b1

Note: "X" means either "0" or "1" is OK.

Figure 10: Analog YUV/RGB Input with Analog Output Mode

Figure 11: Digital 8-bit 601/656 4:2:2 YUV Input with 16bit Digital Output



5725 Key Register Setting		
Register Name	**Address**	**Value**
pad_bout_en	Reg_S0_48[0]	1'b1
pad_bin_enz	Reg_S0_48[1]	1'b1
pad_rout_en	Reg_S0_48[2]	1'b1
pad_rin_enz	Reg_S0_48[3]	1'b1
pad_gout_en	Reg_S0_48[4]	1'b1
pad_gin_enz	Reg_S0_48[5]	1'b0
pad_ckout_enz	Reg_S0_49[1]	1'b0
pad_sync_out_enz	Reg_S0_49[2]	1'b0
pad_blk_out_enz	Reg_S0_49[3]	1'b0
vds_do_16b_en	Reg_S3_50[7]	1'b0
out_blank_sel_0	Reg_S0_50[0]	1'b1
if_sel_adc_sync	Reg_S1_28[2]	1'b0
if_sel_656	Reg_S1_00[3]	1'b1
if_sel16bit	Reg_S1_00[4]	1'b0
if_sel24bit	Reg_S1_01[7]	1'b0

Note: "X" means either "0" or "1" is OK.

Input Pin	Description	Output Pin	Description
VG[7:0]	Digital YUV data input	VB[7:0]	Digtial UV data output
PCLKIN	Pixel clock input	VR[7:0]	Digital Y data output
HSIN1	Video H-sync input	HSOUT	Video H-sync output
VSIN1	Video V-sync input	VSOUT	Video V-sync output
		CLKOUT	Video display clock output
		VBOUT	Display enable output for LCD

System Solution 6: Analog RGB/YUV Input with 16bit Digital Output Mode

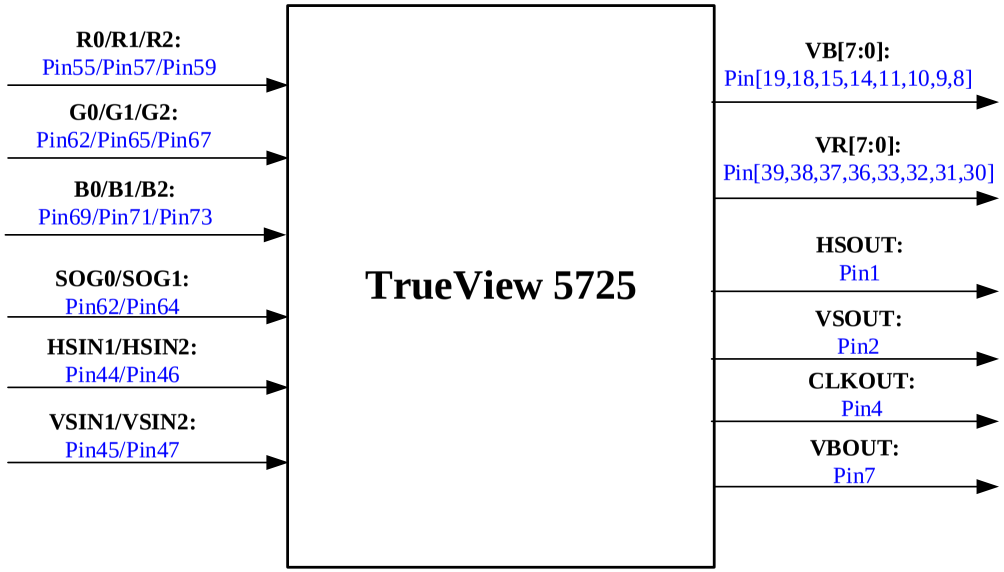


Figure 12: Analog RGB/YUV Input with 16bit Digital Output Mode

5725 Key Register Setting		
Register Name	**Address**	**Value**
pad_bout_en	Reg_S0_48[0]	1'b1
pad_bin_enz	Reg_S0_48[1]	1'b 1
pad_rout_en	Reg_S0_48[2]	1'b 1
pad_rin_enz	Reg_S0_48[3]	1'b 1
pad_gout_en	Reg_S0_48[4]	X
pad_gin_enz	Reg_S0_48[5]	X
pad_ckout_enz	Reg_S0_49[1]	1'b 0
pad_sync_out_enz	Reg_S0_49[2]	1'b 0
pad_blk_out_enz	Reg_S0_49[3]	1'b 0
vds_do_16b_en	Reg_S3_50[7]	1'b 1
out_blank_sel_0	Reg_S0_50[0]	1'b 1
if_sel_adc_sync	Reg_S1_28[2]	1'b 1
if_sel_656	Reg_S1_00[3]	X
if_sel16bit	Reg_S1_00[4]	X
if_sel24bit	Reg_S1_01[7]	1'b 1

Input Pin	Description	Output Pin	Description
R0/R1/R2	Analog R/V input of CHN0/1/2	VB[7:0]	Digtial UV data output
G0/G1/G2	Analog G/Y input of CHN0/1/2	VR[7:0]	Digital Y data output
B0/B1/B2	Analog B/U input of CHN0/1/2	HSOUT	Video H-sync output
SOG0/SOG1	Analog SOG/Y input of CHN1/2	VSOUT	Video V-sync output
HSIN1/HSIN2	Video H-sync input 1/2*	CLKOUT	Video display clock output
VSIN1/VSIN2	Video V-sync input 1/2*	VBOUT	Display enable output for LCD

Note: "X" means either "0" or "1" is OK.

Note*: HSIN1/VSIN1 and HSIN2/VSIN2 could be programmed for analog channel 0/1/2

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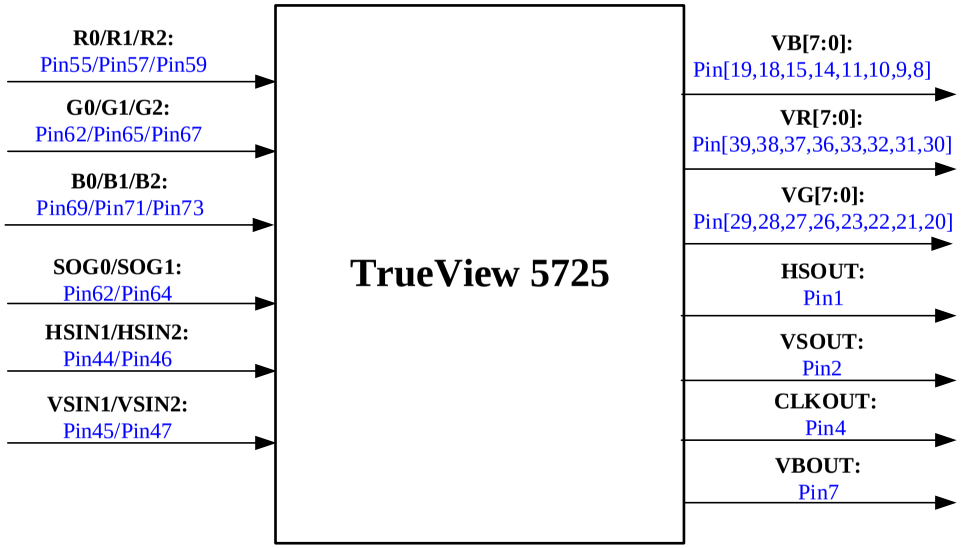
System Solution 7: Analog RGB/YUV Input with 24bit Digital Output Mode



5725 Key Register Setting		
Register Name	**Address**	**Value**
pad_bout_en	Reg_S0_48[0]	1'b1
pad_bin_enz	Reg_S0_48[1]	1'b1
pad_rout_en	Reg_S0_48[2]	1'b1
pad_rin_enz	Reg_S0_48[3]	1'b1
pad_gout_en	Reg_S0_48[4]	1'b1
pad_gin_enz	Reg_S0_48[5]	1'b1
pad_ckout_enz	Reg_S0_49[1]	1'b0
pad_sync_out_enz	Reg_S0_49[2]	1'b0
pad_blk_out_enz	Reg_S0_49[3]	1'b0
vds_do_16b_en	Reg_S3_50[7]	1'b0
out_blank_sel_0	Reg_S0_50[0]	1'b1
if_sel_adc_sync	Reg_S1_28[2]	1'b1
if_sel_656	Reg_S1_00[3]	1'b0
if_sel16bit	Reg_S1_00[4]	X
if_sel24bit	Reg_S1_01[7]	1'b1

Figure 13: Analog RGB/YUV Input with 24bit Digital Output Mode

Input Pin	Description	Output Pin	Description
R0/R1/R2	Analog R/V input of CHN0/1/2	VB[7:0]	Digtial R/V data output
G0/G1/G2	Analog G/Y input of CHN0/1/2	VG[7:0]	Digtial G/Y data output
B0/B1/B2	Analog B/U input of CHN0/1/2	VR[7:0]	Digital B/U data output
SOG0/SOG1	Analog SOG/Y input of CHN1/2	HSOUT	Video H-sync output
HSIN1/HSIN2	Video H-sync input 1/2*	VSOUT	Video V-sync output
VSIN1/VSIN2	Video V-sync input 1/2*	CLKOUT	Video display clock output
		VBOUT	Display enable output for LCD

Note*: HSIN1/VSIN1 and HSIN2/VSIN2 could be programmed for analog channel 0/1/2

Note: "X" means either "0" or "1" is OK.

BOARD MEMORY CONNECTION:

Figure 14: THREE 1MX16X2BANK MEMORY (1)

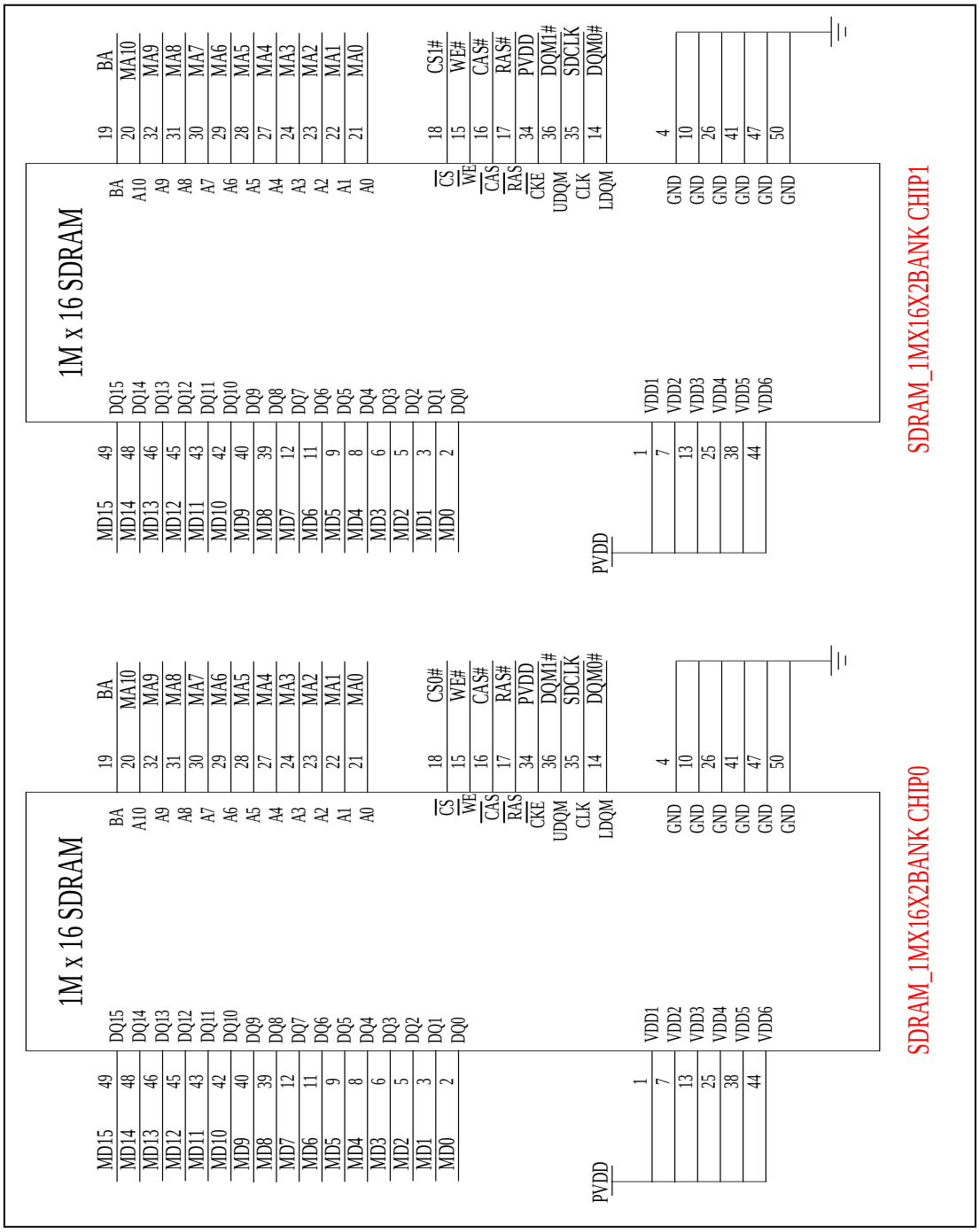


Figure 15: THREE 1MX16X2BANK MEMORY (2)

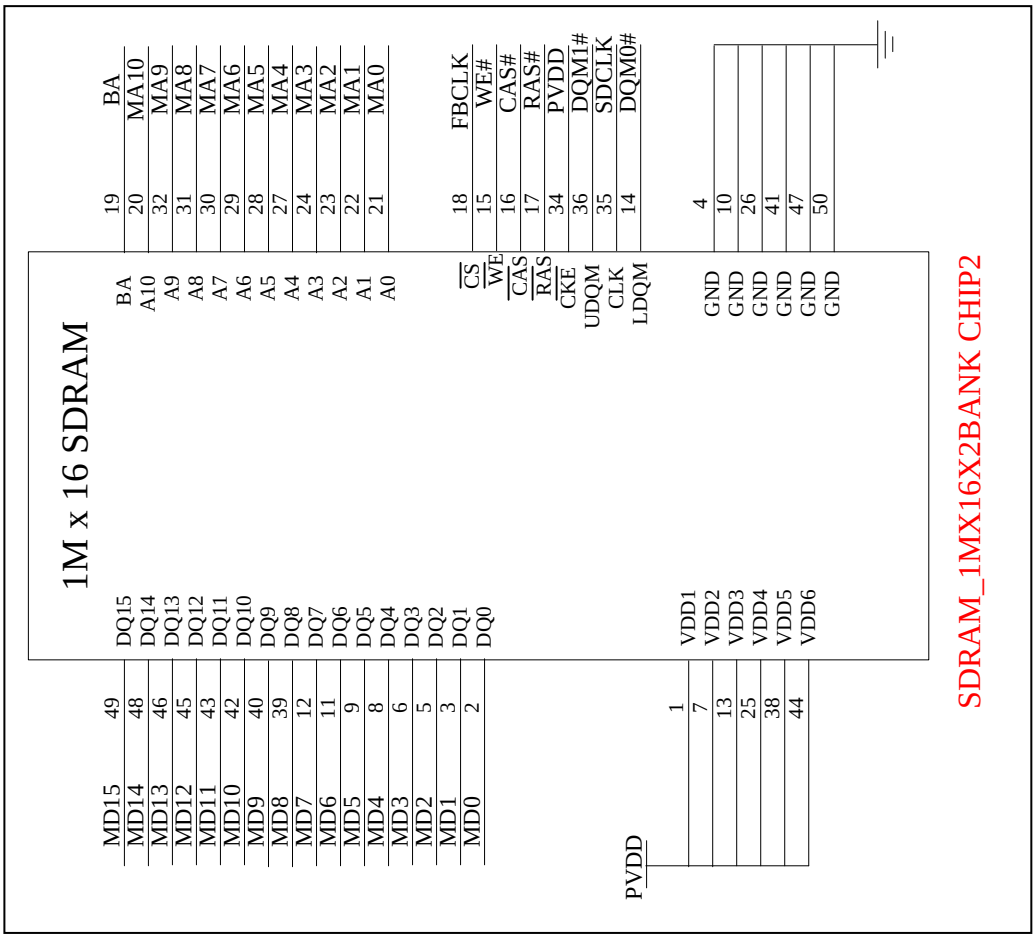


Figure 16: ONE 1MX16X4BANK MEMORY

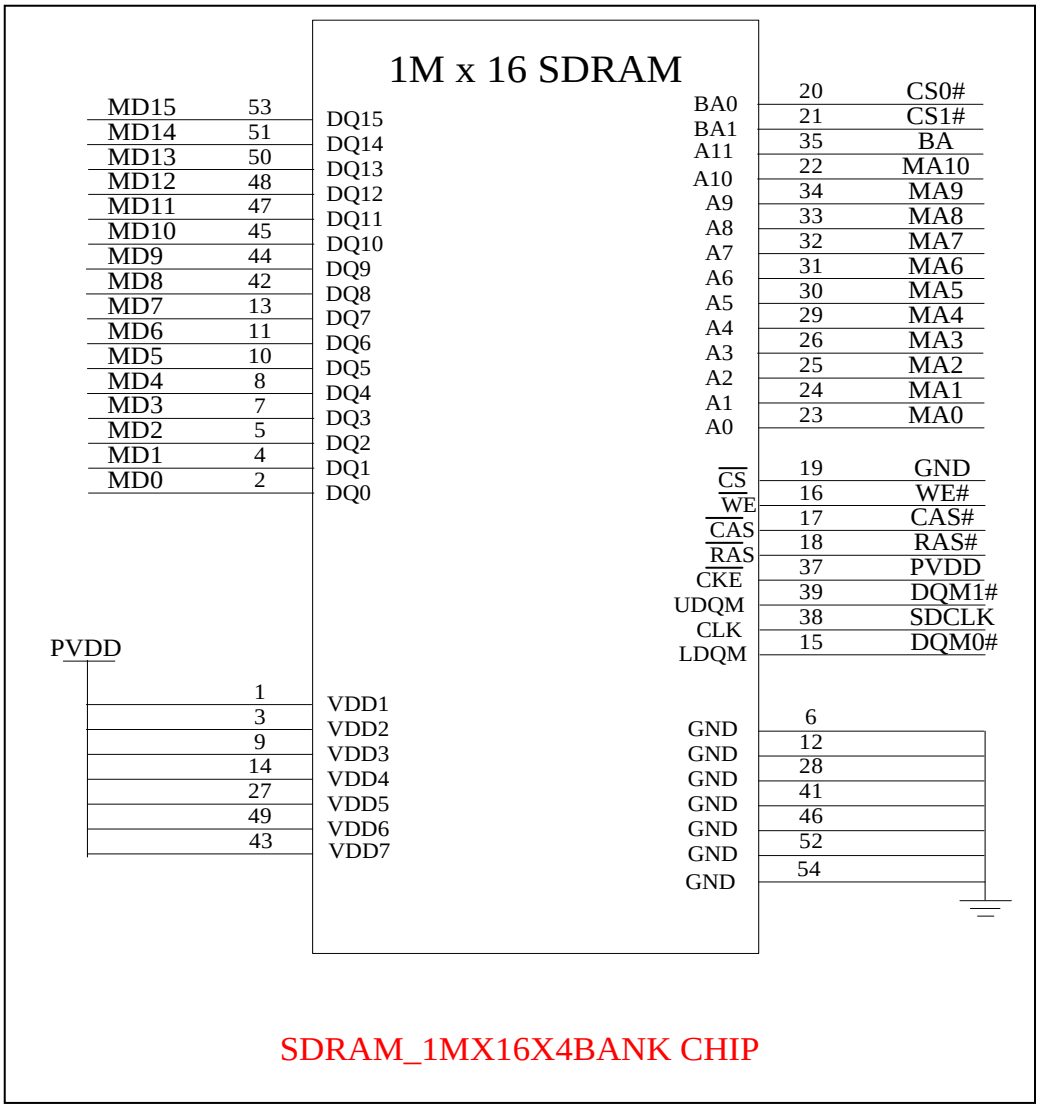


Figure 17: ONE 512KX32X4BANK MEMORY

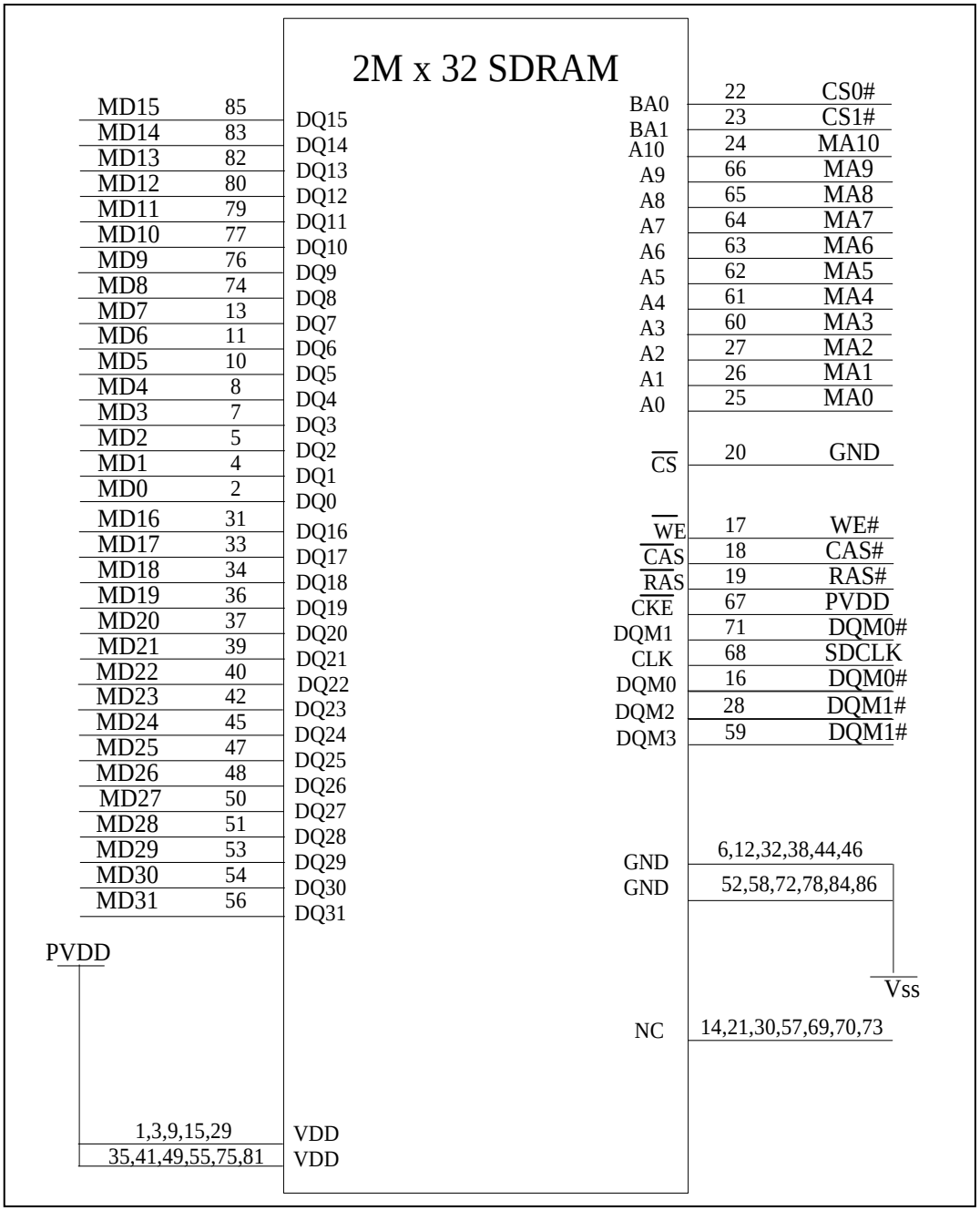
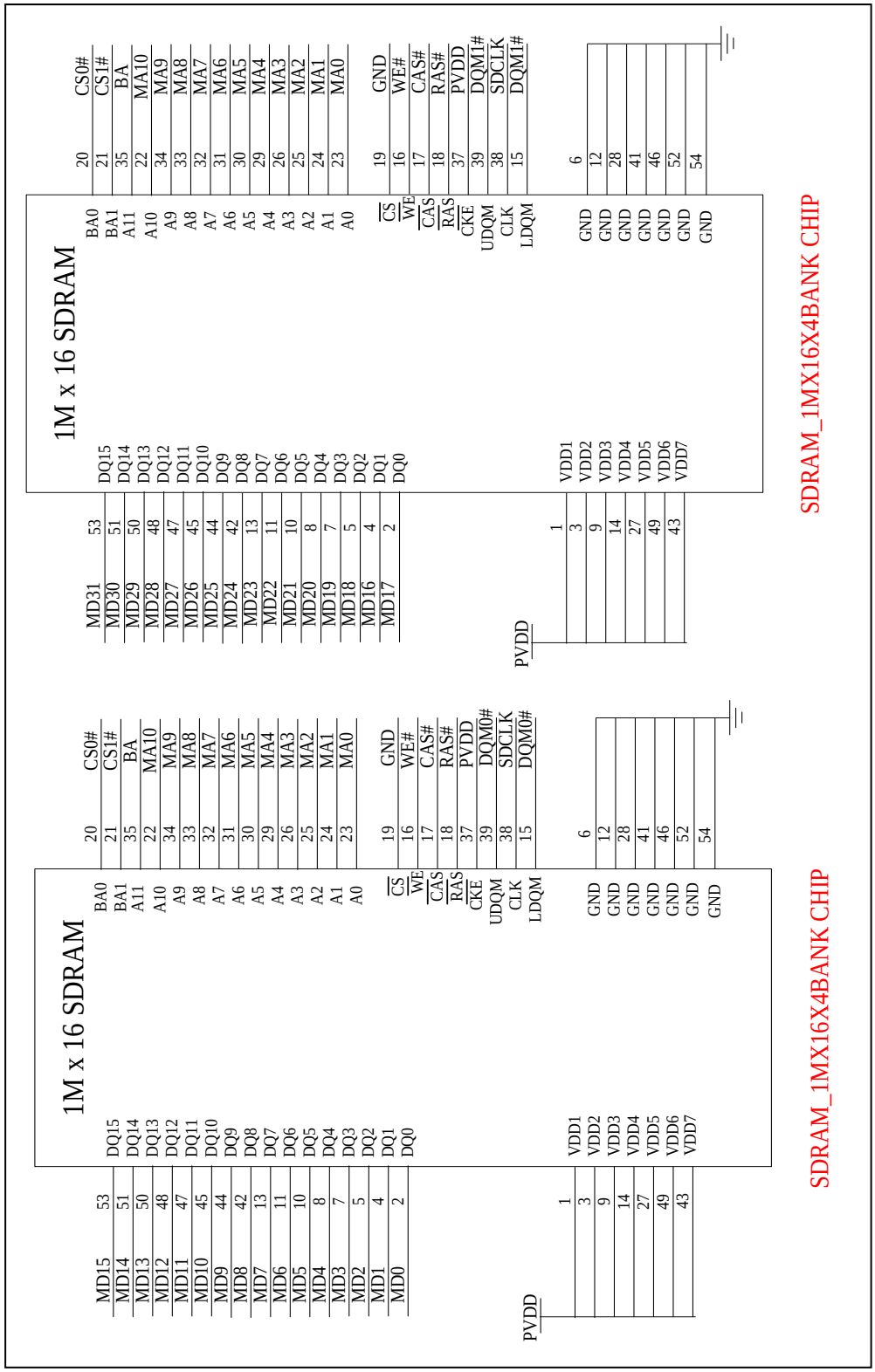


Figure 18: TWO 1MX16X4BANK MEMORY



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Table 12: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Conditions
3.3V Power Supply Voltage (Reference to Ground)	VDD[1]	- 0.3	4.0	V	
1.8V Power Supply Voltage (Reference to Ground)	VCC	- 0.3	2.2	V	
Voltage on any input	V_I	- 0.3	VDD+0.3	V	
Storage Temperature	T_S	- 40	125	℃	
Operating temperature	T_o	0	70	℃	

Warning: Stressing the device beyond the "Absolute maximum Ratings" may cause permanent damage.

Notes

1. *TV5725's 3.3V power supply : PVDD, DAVD, PAVD, AVD_PLL, AVD_REF, AVD_R, AVD_G, AVD_B.*

DC CHARACTERISTICS

Table 13: DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Comments
1.8V Power Supply Voltage (1.8V±5%)	VCC	1.71		1.89	V	1.8V Operation
3.3V Power Supply Voltage (3.3V±5%)	PVDD, DAVD, PAVD, AVD_PLL, AVD_REF, AVD_R, AVD_G, AVD_B	3.135		3.465	V	3.3V Operation
1.8V Supply Current[1.a] (VCC)	IVCC		320		mA	
3.3V Supply Current[1.a] (PVDD, PAVD, AVD_PLL)	IVDD33		100		mA	
3.3V Supply Current[1.b] (AVD_REF, AVD_R, AVD_G, AVD_B)	IAVD		240		mA	
3.3V Supply Current[1.c] (DAVD)	IDAVD		85		mA	
Input Low Voltage	VIL	0		0.8	V	
Input High Voltage	VIH	2.0		Vcc + 0.3	V	
Schmitt Input Low Voltage[2]	VILS	0		1.0	V	
Schmitt Input High Voltage[2]	VIHS	2.4		Vcc + 0.3	V	
Output Low Voltage	VOL			0.4	V	IOL = 8mA
Output High Voltage	VOH	2.4			V	IOH = -8mA
Input Capacitance	CIN		7		pF	
Output Capacitance	COUT		7		pF	

Notes

1. Current measured condition:

a. @ HD 1080i, 74.25MHz input, SOG, 162MHz 32bit memory, 108MHz Display clock, VCC is 1.8V.
b. @ UXGA 60Hz, power supply is 3.3V.
c. For VESA Video Levels, the R_{iref} in the board is 160ohms. The output load is double terminated with 75ohms and 10pf per channel. Full-scale for all four channels is 0.7V, power supply is 3.3V. Measurement temperature is 25^0C. This is a preliminary measurement and is subject to change by Tvia, Inc.

2. Schmitt trigger PADs (Total: 41 Pads):

HSOUT, VSOUT

CLKOUT

HBOUT, VBOUT

VB[0:7]

VG[0:7]

VR[0:7]

PCLKIN

SCLSA

HSIN1, VSIN1, HSIN2, VSIN2

RSTN

GPIO

HALF

MBA

MCS1#

FBCLK

AC CHARACTERISTICS

Figure 19: Video Input Port AC Timing

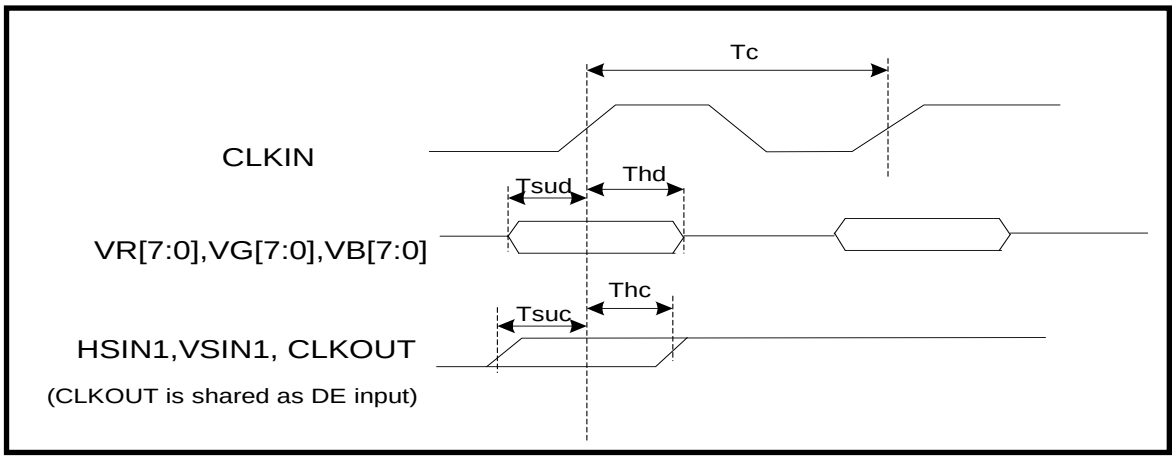


Table 14: Video Input Port AC Timing

Parameter	Symbol	Min	Typ	Max	Units	Conditions
VR[7:0], VG[7:0], VB[7:0] Setup Time to CLKIN	Tsud	2			ns	
VR[7:0], VG[7:0], VB[7:0] Hold Time to CLKIN	Thd	5			ns	
HSIN1, VSIN1, CLKOUT Setup Time to CLKIN	Tsuc	2			ns	
HSIN1, VSIN1, CLKOUT Hold Time to CLKIN	Thc	6			ns	
CLKIN Frequency	1/Tmc			80	MHz	

Figure 20: Video Output Port AC timing

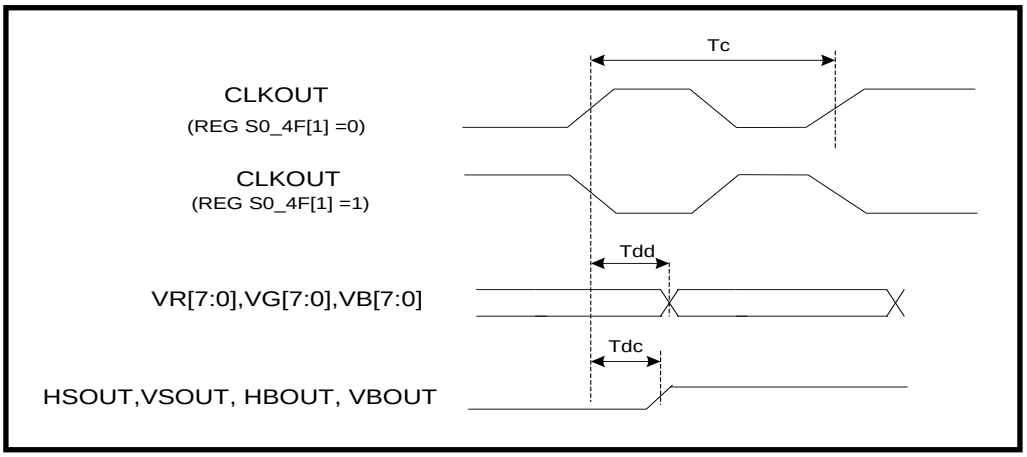


Table 15: Video Output Port AC timing

Parameter	Symbol	Min	Typ	Max	Units	Conditions
VR[7:0], VG[7:0], VB[7:0] Delay Timing from CLKOUT	Tdd	-1		1.5	ns	20pF load
HSOUT, VSOUT, HBOUT, VBOUT Delay Timing from CLKOUT	Thd	-1		2.5	ns	20pF load
CLKOUT Frequency	1/Tmc			108	MHz	20pF load

MEMORY INTERFACE AC CHARACTERISTICS

Figure 21: Memory Interface AC Input timing

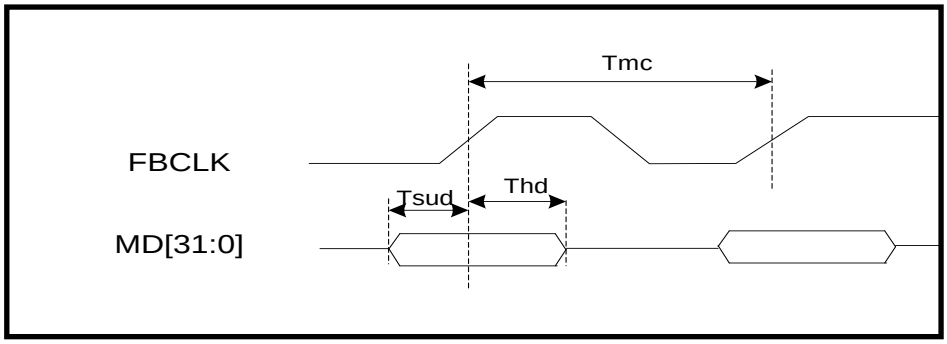


Table 16: Memory Interface AC Input timing

Parameter	Symbol	Min	Typ	Max	Units	Conditions
MD[31:0] Setup Time to FBCLK	Tsud	2.0			ns	
MD[31:0] Hold Time to FBCLK	Thd	1.5			ns	
FBCLK Frequency	1/Tmc			162	MHz	

Figure 22: Memory Interface AC output timing

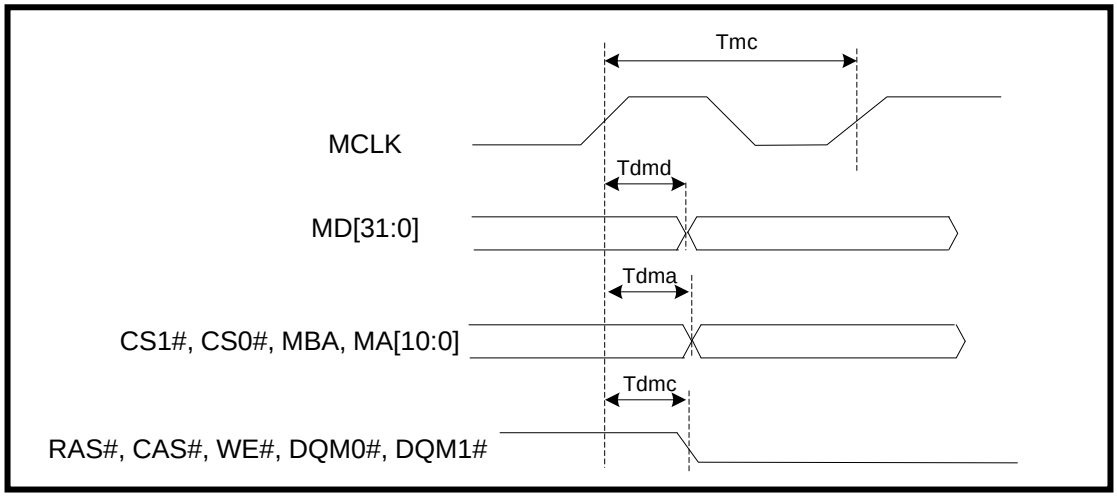
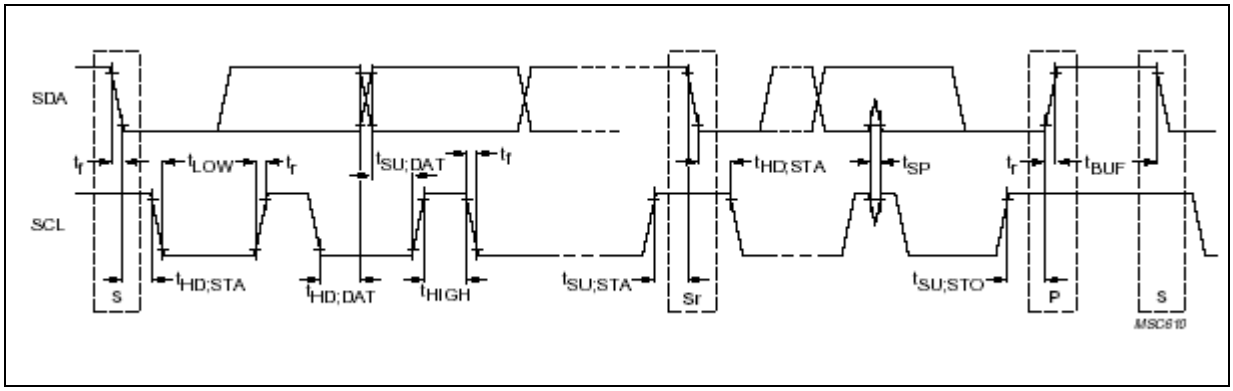


Table 17: Memory Interface AC output timing

Parameter	Symbol	Min	Typ	Max	Units	Conditions
MD[31:0] Delay Time from MCLK	Tdmd	3.7		5.4	ns	20pF load
CS1#, CS0#, MBA, MA[10:0] Delay Time from MCLK	Tdma	3.7		5.4	ns	20pF load
RAS#, CAS#, WE#, DQM0#, DQM1# Delay Time from MCLK	Tdmc	3.7		5.4	ns	20pF load
MCLK Frequency	1/Tmc			162	MHz	20pF load

Figure 23: Definition of timing for F/S-mode devices on the I²C-bus



**** Figure 7 Referenced document:***

Philips Semiconductors, "The I²C-BUS Specification, version2.1 ---January 2000"

Page33: Fig.31: Definition of timing for F/S-mode devices on the I²C-bus.

Table 18: Characteristics of the SDA and SCL bus lines for F/S-mode I²C-bus devices

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

Notes:

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
2. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r\,max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.
4. C_b = total capacitance of one bus line in pF.

**** Table 17 Referenced document:***

Philips Semiconductors, "The I²C-BUS Specification, version2.1 ---January 2011"

Page32: Table 5: Characteristics of the SDA and SCL bus lines for F/S-mode I²C-bus devices[1]

DAC CHARACTERISTICS

Table 19: DAC Characteristics

Parameter	Min	Typical	Max	Unit	Notes
Resolutions			10	Bits	
Number of channels		4			
Clock Rate		162		MHz	
INL	-1.0		+1.0	LSB	
DNL	-1.0		+1.0	LSB	
Full Scale Voltage	665	700	770	mV	1, 2
LSB Current		18.2		uA	1
Monotonicity		Guaranteed			
RGB Video Output Rise Time (10-90% of full-scale)		2.6	4.7	ns	3
RGB Video Output Fall Time (10-90% of full-scale)		2.5	4.0	ns	3

NOTES:

1. For VESA Video Levels, the R_{iref} in the board is 160ohms. The output load is double terminated with 75ohms and 10pf per channel. Full-scale for all four channels is 0.7V.
2. For good linearity, the full-scale voltage should be less than 1V when the output load is 75ohms and 10pf per channel.
3. As measured with 37.5ohm and 10pf load.

ADC CHARACTERISTICS

Table 20: ADC Characteristics

Parameter	Min	Typical	Max	Unit	Notes
Resolutions			8	Bits	
Number of channels		3			
Sampling Frequency (Fs)	10		162	MHz	
Full Scale Adjust Range at RGB Inputs	0.5		1	V	1
Reference Voltage		1.24		V	2
INL		+/- 1.2		LSB	
DNL		+/- 0.8		LSB	
No Missing Codes		Guaranteed			

NOTES:

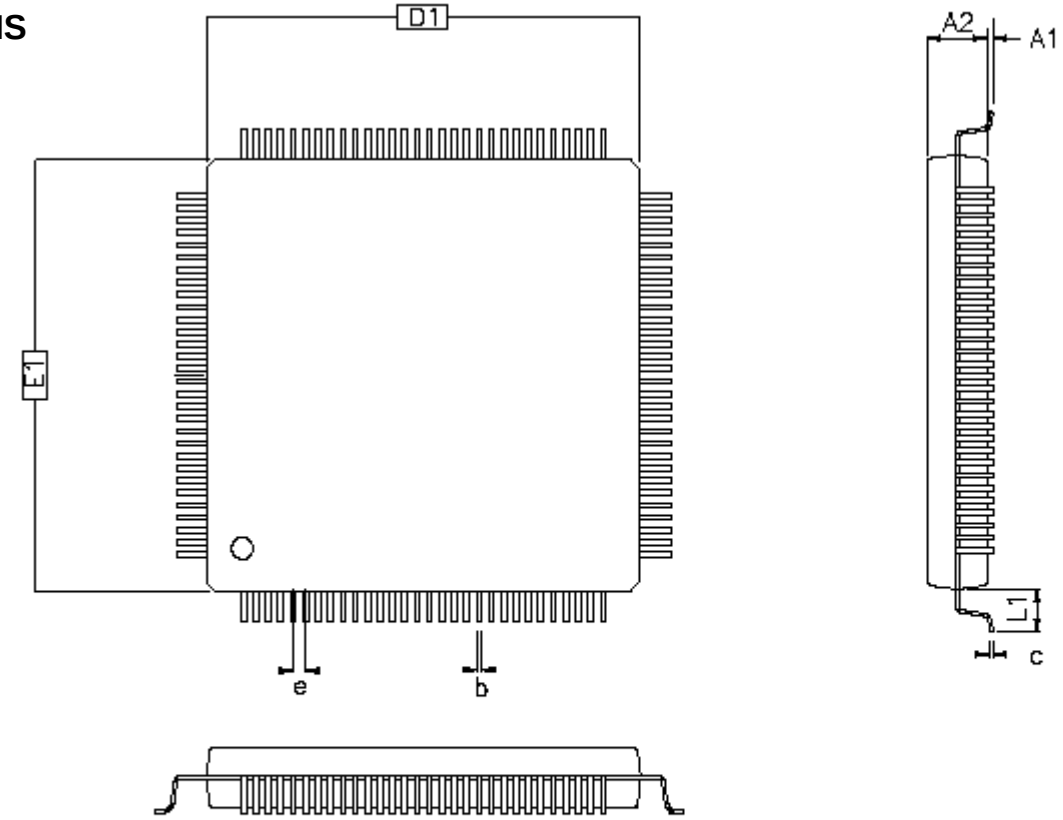
1. Operation with 8-bit gain controller and 7-bit offset controller.
2. Internal reference voltage output.

Figure 24: Package Dimensions for QFP160 Package

PACKAGE DIMENSIONS

In Millimeters

	Min	Typ	Max
A1	0.25		
A2	3.2	3.32	3.6
L1		1.6REF	
b	0.22	0.3	0.38
c	0.09	0.15	0.2
e		0.65 BSC	
D1		28	
E1		28	



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