Features

- Operating voltage: 2.4V~5.5V
- LED display -- 44 row and 8 Columns
- 88×4 bit RAM display data storage
- 16-level PWM brightness control
- Integrated 256kHz RC oscillator
- I²C-bus or 4-wire serial interface
- Data mode & command mode instructions
- Cascade function for extend applications
- Selectable NMOS open drain output driver and PMOS open drain output driver for COM lines
- 64-pin LQFP package

Applications

- Industrial control displays
- Digital clocks, thermometers, counters, electronic meters
- Instrumentation readouts
- Other consumer applications
- LED displays

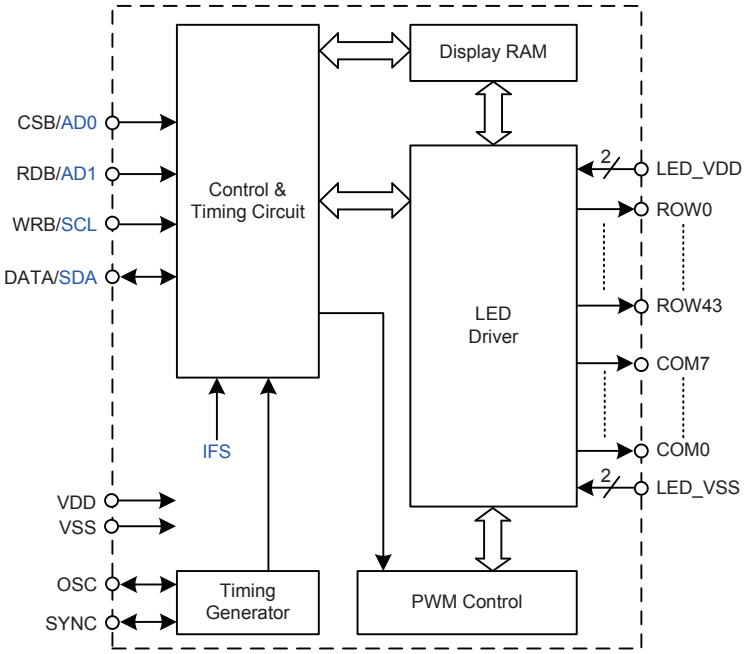
General Description

The HT1635 is a memory mapping LED display controller/driver. The maximum display capacity of the device is 352 patterns composed of 44 rows and 8 commons. The device can generate 16 LED illumination levels using software controlled PWM circuitry. A serial interface is provided to allow the device to receive instructions for its command mode and data mode. Only three or four lines are required to interface the device to a host controller. The display capacity can be easily extended by cascading the devices thus expanding its application possibilities. The device is compatible with most microcontrollers offering easy interfacing via its two serial interfaces, an I²C bus or a 4-wire serial bus.

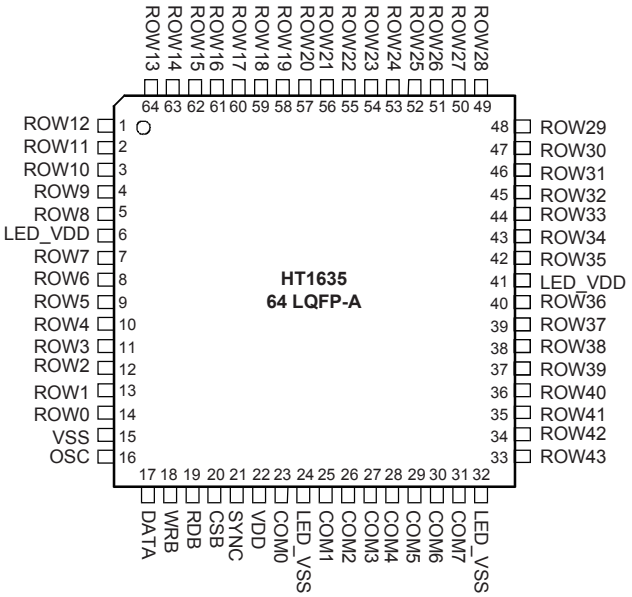
Selection Table

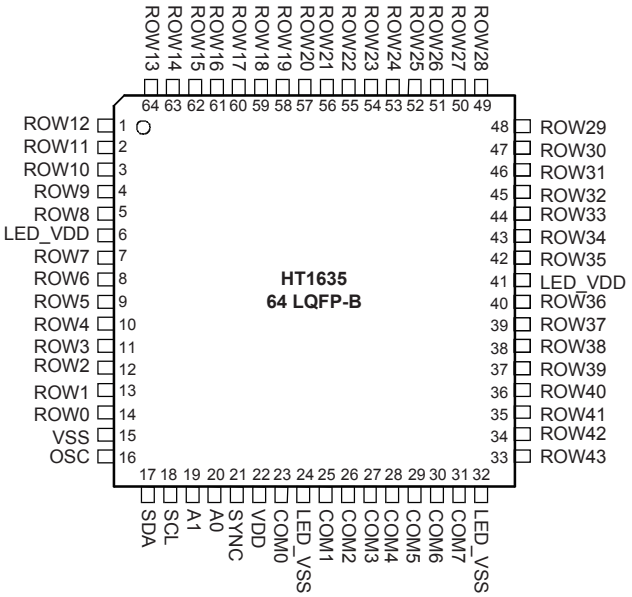
Part Number	Interface
HT1635A	4-wire serial bus
HT1635B	I²C serial bus

Block Diagram



Pin Assignment





Pin Description

Pin Name	I/O	Function
COM0~COM7	O	LED common output lines.
ROW0~ROW43	O	LED row output lines.
LED_VSS	—	Negative power supply for driver circuit, ground.
LED_VDD	—	Positive power supply for driver circuit.
VDD	—	Positive power supply for logic circuit.
VSS	—	Negative power supply for logic circuit, ground.
DATA/SDA	I/O	Serial data input/output pin. Data is input to / comes out from the shift register at rising edge of the clock. • I^2C interface serial data (SDA) Input/Output. NMOS open-drain output • SPI 4-wire interface serial data input/output. Input has pull-high resistor and output is CMOS type.
WRB/SCL	I	Serial clock input pin. • I^2C interface serial clock SCL input. • SPI 4-wire interface WRITE Clock (CLK) input. Connected to pull-high resistor. Data on the DATA line is latched into the device on the rising edge of the WRB signal.
RDB/A1	I	• I^2C interface device address data input pin. • SPI 4-wire interface READ clock input. Connected to pull-high resistor. The device RAM data is clocked out on the falling edge of RDB. The clocked out data will appear on the DATA line. The host controller can use the next rising edge to latch the clocked out data.
CSB/A0	I	• I^2C interface device address data input pin. • Chip select input. Connected to pull-high resistor. When CSB is high, a data and command instruction read from or written to the device is disabled and the serial interface circuit is also reset. If CSB is low data and command instruction transmission between the host controller and the device is enabled.
OSC	I/O	• If the RC MASTER MODE command is programmed, the system clock is sourced from the internal RC oscillator and the system clock is output on the OSC pin. • If the SLAVE MODE or EXT CLK MASTER MODE command is programmed, the system clock is sourced from an external clock on the OSC pin.
SYNC	I/O	• If the RC MASTER MODE or EXT CLK MASTER MODE command is programmed, the synchronous signal is output on the SYNC pin. • If the SLAVE MODE command is programmed, the synchronous signal is input on the SYNC pin.

Absolute Maximum Ratings

Supply Voltage .....V_{SS}-0.3V to V_{SS}+6.0V

Input Voltage.....V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature .....-50˚C to 125˚C

Operating Temperature.....-40˚C to 85˚C

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

V_{DD}=2.4V~5.5V; Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	5	5.5	V
I_{DD}	Operating Current	5	No load, LED ON, On-chip RC oscillator	—	0.3	0.6	mA
I_{STB}	Standby Current	5	No load, Power down mode	—	1	2	μA
V_{IL}	Input Low Voltage	5	DATA, WRB, RDB, SDA, SCL, CSB, OSC, SYNC	0	—	$0.3V_{DD}$	V
V_{IH}	Input High Voltage	5	DATA, WRB, RDB, SDA, SCL, CSB, OSC, SYNC	$0.7V_{DD}$	—	5	V
I_{OL1}	OSC, SYNC, DATA, SDA	5	V_{OL}=0.5V	18	25	—	mA
I_{OH1}	OSC, SYNC, DATA	5	V_{OH}=4.5V	-10	-13	—	mA
I_{OL2}	ROW sink current	5	V_{OL}=0.5V	10	13	—	mA
I_{OH2}	ROW source current	5	V_{OH}=4.5V	-50	-70	—	mA
I_{OL3}	COM Sink Current	5	V_{OL}=0.5V	250	400	—	mA
I_{OH3}	COM Source Current	5	V_{OH}=4.5V	-45	-60	—	mA
R_{PH}	Pull-high Resistor	5	DATA, WRB, RDB, CSB	18	27	40	kΩ

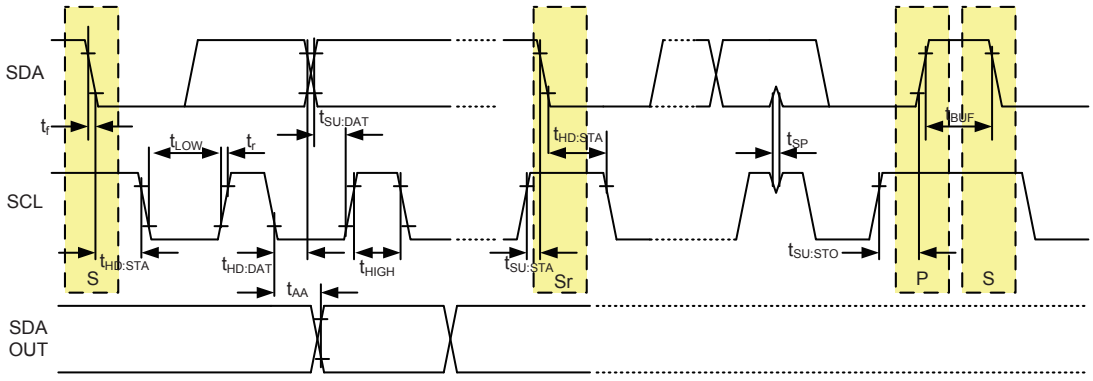
A.C. Characteristics

I²C serial bus

V_{DD}=2.4V~5.5V; Ta=25°C

Symbol	Parameter	Condition	V_{DD}=2.4V to 5.5V		V_{DD}=3.0V to 5.5V		Unit
			Min.	Max.	Min.	Max.	
f_{SCL}	Clock frequency	—	—	100	—	400	kHz
t_{BUF}	bus free time	Time in which the bus must be free before a new transmission can start	4.7	—	1.3	—	μs
$t_{HD:STA}$	Start condition hold time	After this period, the first clock pulse is generated	4	—	0.6	—	μs
t_{LOW}	SCL Low time	—	4.7	—	1.3	—	μs
t_{HIGH}	SCL High time	—	4	—	0.6	—	μs
$t_{SU:STA}$	Start condition setup time	Only relevant for repeated START condition.	4.7	—	0.6	—	μs
$t_{HD:DAT}$	Data hold time	—	0	—	0	—	ns
$t_{SU:DAT}$	Data setup time	—	250	—	100	—	ns
t_R	SDA and SCL rise time	Note	—	1	—	0.3	μs
t_F	SDA and SCL fall time	Note	—	0.3	—	0.3	μs
$t_{SU:STO}$	Stop condition set-up time	—	4	—	0.6	—	μs
t_{AA}	Output Valid from Clock	—	—	3.5	—	0.9	μs
t_{SP}	Input Filter Time Constant (SDA and SCL Pins)	Noise suppression time	—	20	—	20	ns

Note: These parameters are periodically sampled but not 100% tested.



I²C Bus Timing

4-wire Serial Bus

V_{DD}=2.4V~5.5V; Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{sys}	System Clock	5V	On-chip RC oscillator	230	256	282	kHz
f_{LED}	LED frame rate	5V	1/8 duty	—	f_{SYS}/2624	—	Hz
f_{clk1}	Serial Data Clock (WRB pin)	5V	Duty cycle 50%	—	—	1	MHz
f_{clk2}	Serial Data Clock (RDB pin)	5V	Duty cycle 50%	—	—	500	kHz
t_{cs}	Serial Interface Reset Pulse Width	—	CSB	250	—	—	ns
t_{clk}	WRB, RDB Input Pulse Width	5V	Write mode	0.5	—	—	μs
			Read mode	1	—	—	
t_r, t_f	Rise/Fall Time for WRB, RDB signal (Figure 1)	—	—	—	50	100	ns
t_{su}	Setup Time for DATA to WRB, RDB Clock Width (Figure 2)	—	—	50	100	—	ns
t_h	Hold Time for DATA to WRB, RDB Clock Width (Figure 2)	—	—	100	200	—	ns
t_{su1}	Setup Time for CSB to WRB, RDB, Clock Width (Figure 3)	—	—	200	300	—	ns
t_{h1}	Hold Time for CSB to WRB, RDB, Clock Width (Figure 3)	—	—	100	200	—	ns
t_{od}	Data Output Delay Time (Figure 4)	—	—	—	100	200	ns
t_{OFF}	V_{DD} OFF Times (Figure 5)	—	VDD drop down to 0V	10	—	—	ms
t_{SR}	V_{DD} Rising Slew Rate (Figure 5)	—	—	0.1	—	0.8	V/ms
t_{RSTD}	Delay Time after Reset (Figure 5)	—	—	1	—	—	ms

Note: 1. If the conditions of the Power on Reset timing are not satisfied during power ON/OFF, the internal Power on Reset (POR) circuit will not operate normally.

2. During normal operation, if the VDD drops below the minimum voltage as defined in the operating voltage spec, then the conditions for the Power on Reset timing must also be satisfied. This means that VDD must drop to 0V and remain there for 20ms (min.) before rising to the normal operating voltage.

3. Data transfers on the I²C-bus or 4-wire serial bus should be avoided for 1 ms following a power-on to allow the reset sequence to complete

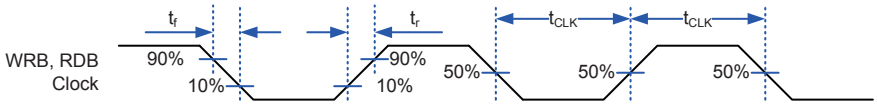


Figure 1

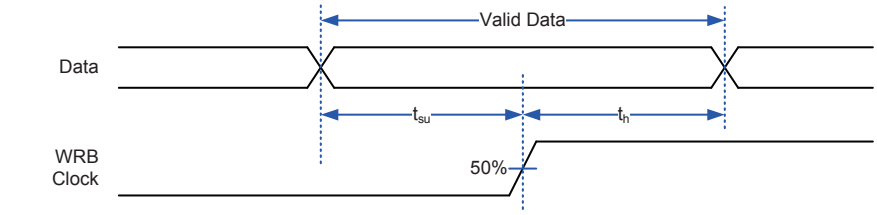


Figure 2

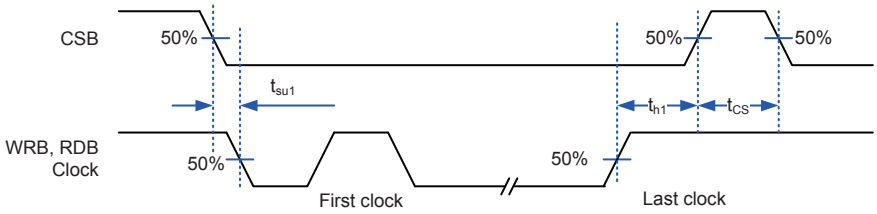


Figure 3

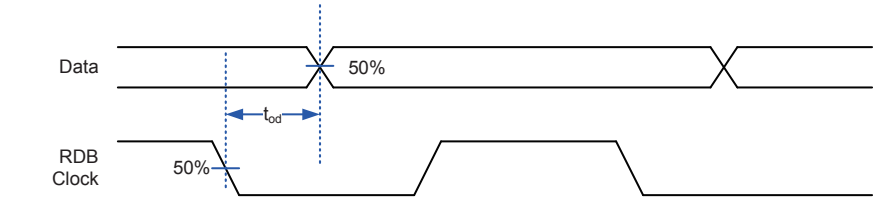


Figure 4

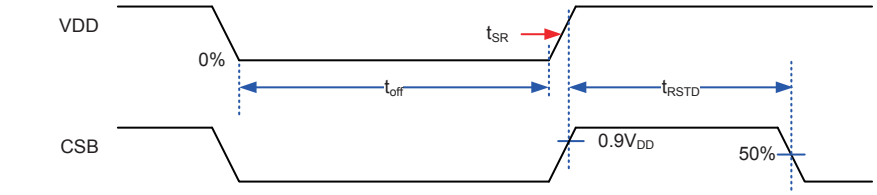


Figure 5

Functional Description

Power-on Reset

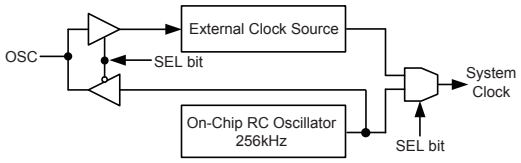
After power is applied the device will be initialised by an internal power-on reset circuit. The status of the internal circuits after initialisation is as follows:

- System Oscillator will be off
- COM0~COM7 outputs status is high impedance.
- The row CMOS outputs will all be low
- The LED display will be in an off state
- Dimming is set to 16/16duty
- The Blinking function will be in an state

Data transfers on the I^2C-bus or 3-wire serial bus should be avoided for 1 ms following a power-on to allow the reset initialisation operation to complete.

System Oscillator

The system clock is used to generate the time base clock frequency LED-driving clock. The clock may be sourced from an on-chip 256kHz RC oscillator or from an external clock using software setups. After the SYS DIS command is executed, the system clock will stop and the LED duty cycle generator will turn off. This command is however available only for the on-chip RC oscillator. Once the system clock stops the LED display will become blank and the time base will also stop functioning. The LED OFF command is used to turn the LED duty cycle generator off. After the LED duty cycle generator switches off by issuing the LED OFF command, using the SYS DIS command will reduce the power consumption, allowing it to operate as a system power down command. However if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor execute the power down mode. The crystal oscillator option can also be used where an external frequency source is connected to the OSC pin. In this case, the system will fail to enter the power down mode, similar to the case for the external clock source operation. After an initial system power on, the device will be in the SYS DIS state.



System Oscillator Configuration

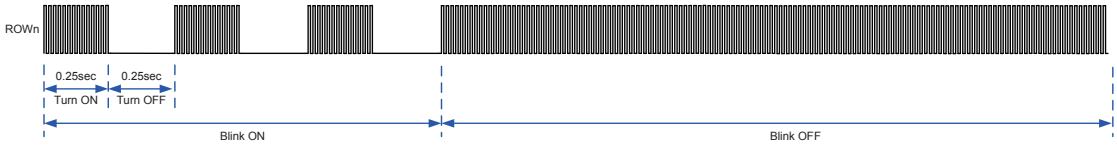
Display Data Address Pointer

The address mechanism for the display RAM is implemented using the address pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialisation of the address pointer by the address pointer command.

Blinker

The device contains a versatile blinking function. The whole display can be made to flash at frequencies selected by the Blink command. The blinking frequencies are integer multiples of the system frequency. The ratios between the system oscillator and the blinking frequencies depend upon the mode in which the device is operating, as follows:

- Blinking frequency = 2Hz



Example of Waveform for Blinker

Display Memory – RAM Structure

- The display RAM is a static 88×4-bit RAM which stores the LED data. Logic "1" in the RAM bit-map indicates an "on" state of the corresponding LED Row. Similarly, a logic 0 indicates the "off" state.
- There is a one-to-one correspondence between the RAM addresses and the Row outputs, and between the individual bits of a RAM word and the column outputs. The following shows the mapping from the RAM to the LED pattern:

	COM7	COM6	COM5	COM4		COM3	COM2	COM1	COM0	
ROW0					01H					00H
ROW1					03H					02H
ROW2					05H					04H
ROW3					07H					06H
ROW4					09H					08H
ROW5					0BH					0AH
ROW6					0DH					0CH
ROW7					0FH					0EH
ROW8					11H					10H
ROW9					13H					12H
ROW10					15H					14H
ROW11					17H					16H
ROW12					19H					18H
ROW13					1BH					1AH
ROW14					1DH					1CH
ROW15					1FH					1EH
ROW16					21H					20H
ROW17					23H					22H
ROW18					25H					24H
ROW19					27H					26H
ROW20					29H					28H
ROW21					2BH					2AH
ROW22					2DH					2CH
ROW23					2FH					2EH
ROW24					31H					30H
ROW25					33H					32H
ROW26					35H					34H
ROW27					37H					36H
ROW28					39H					38H
ROW29					3BH					3AH
ROW30					3DH					3CH
ROW31					3FH					3EH
ROW32					41H					40H
ROW33					43H					42H
ROW34					45H					44H
ROW35					47H					46H
ROW36					49H					48H
ROW37					4BH					4AH
ROW38					4DH					4CH
ROW39					4FH					4EH
ROW40					51H					50H
ROW41					53H					52H
ROW42					55H					54H
ROW43					57H					56H
	D3	**D2**	**D1**	**D0**	**Addr / Data**	**D3**	**D2**	**D1**	**D0**	**Addr / Data**

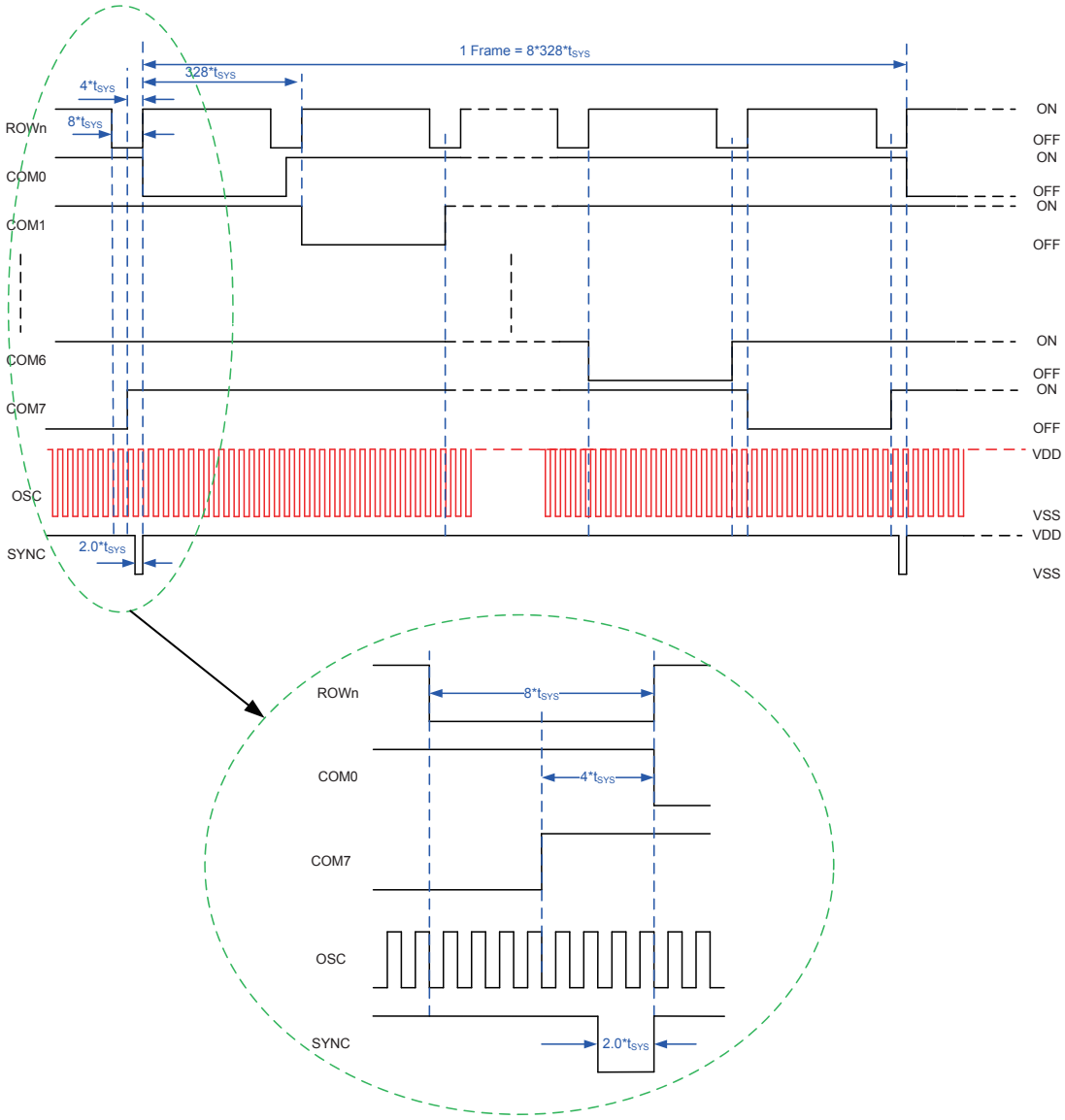
44ROW & 8COM for 88 × 4 Display RAM

Note: The LCD display RAM address is specified by the Address Set command. The address will be automatically incremented by one after the 4-bit data is shifted in.

LED Driver

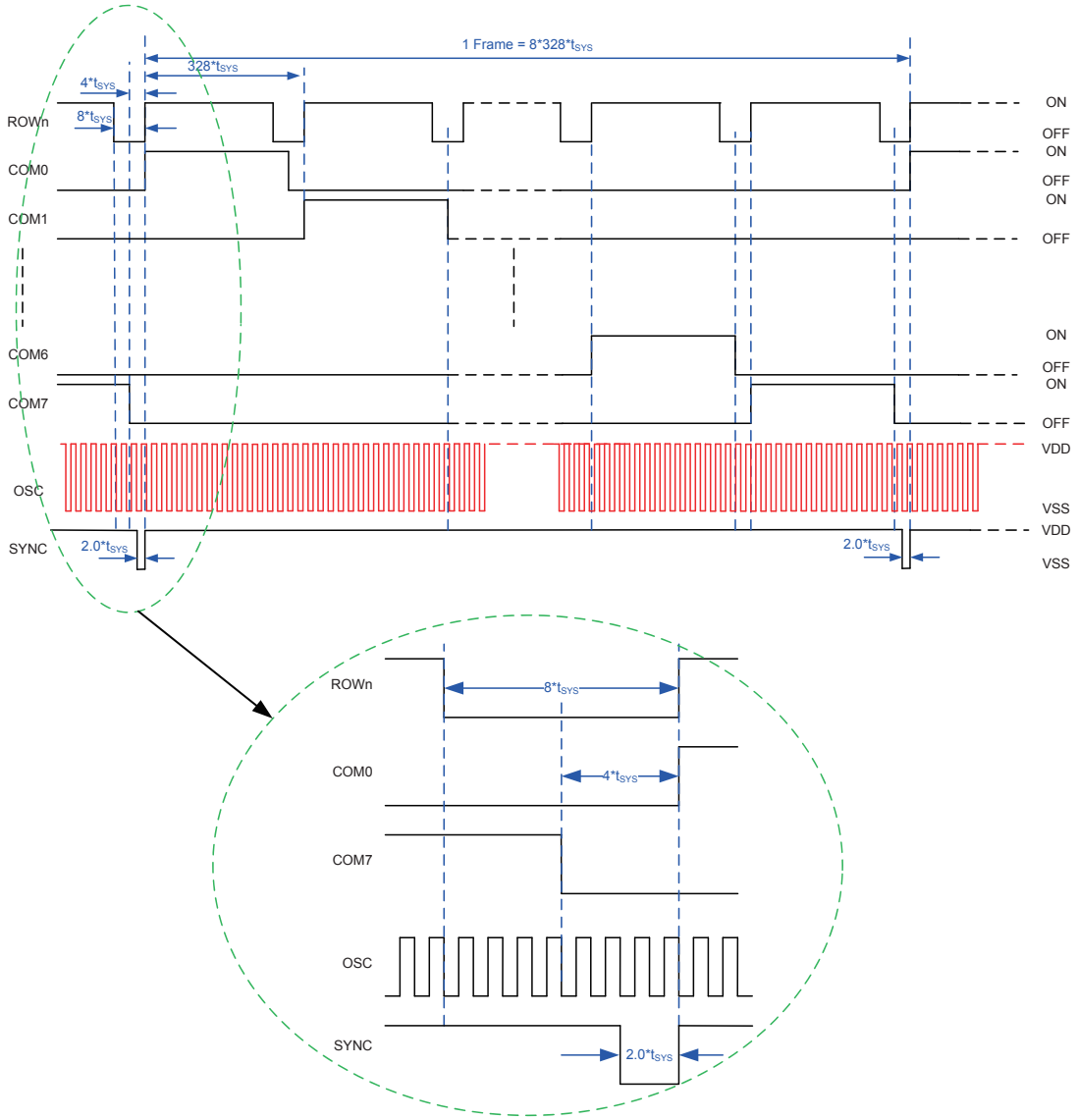
The device includes a 352 (44 × 8) pattern LED driver. This can be setup in a 44x8 format where the COM outputs can be configured as N-MOS open drain outputs or as P-MOS open drain outputs using software setups. This feature allows the device to be used in multiple LED applications. The LED drive mode waveforms and scanning is as follows:

1. N-MOS Open Drain for 44×8 Driver Mode



Note: $t_{SYS}=1/f_{SYS}$

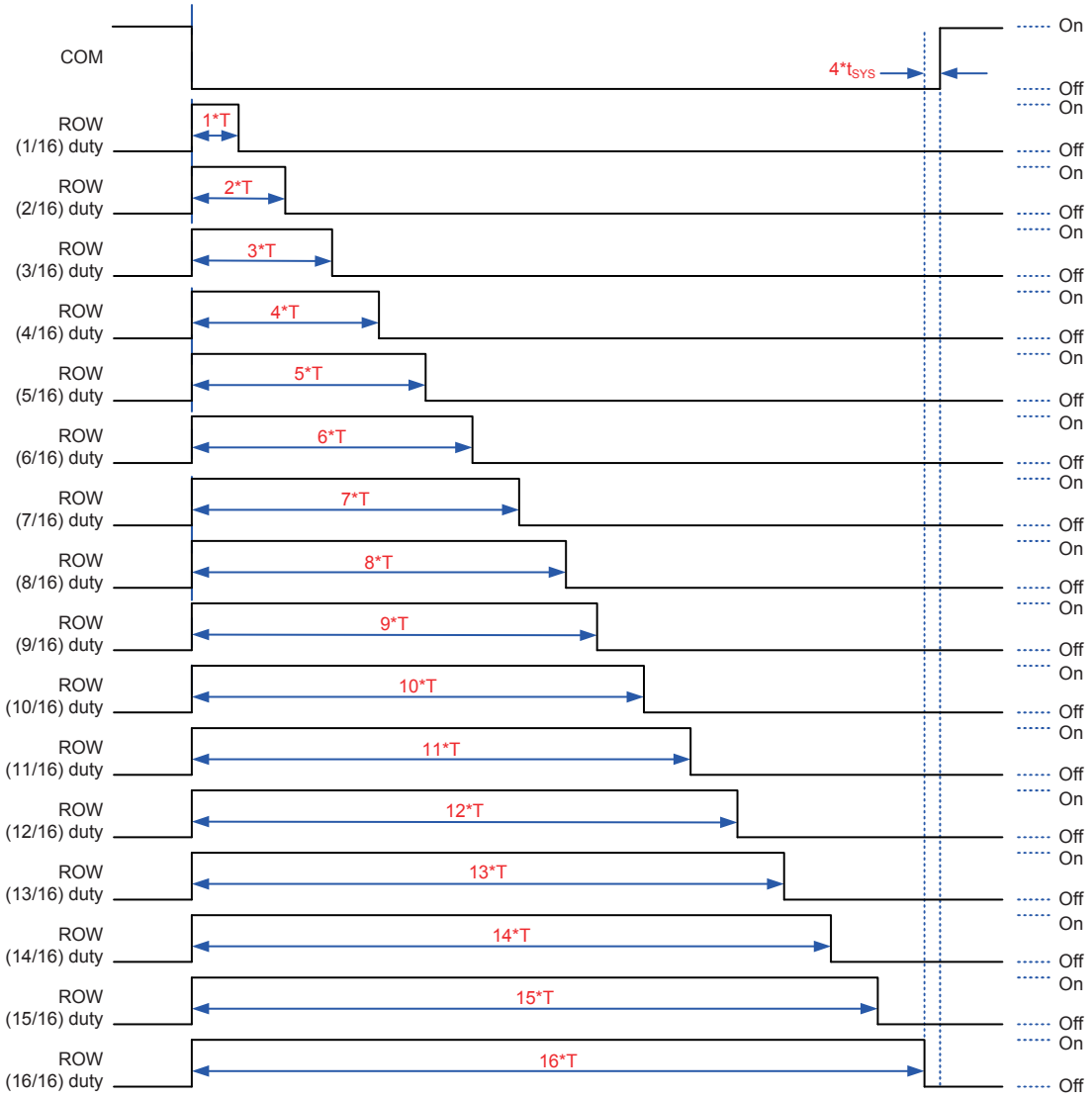
2. P-MOS Open Drain for 44×8 Driver Mode



Note: $t_{SYS}=1/f_{SYS}$

Digital Dimming

The device contains versatile dimming functions. The complete display can be dimmed using pulse width modulation techniques for the ROW driver with the Dimming command. The relationship between the ROW and COM digital dimming duty times are shown in the accompanying diagram.



Note: $T=20\times t_{SYS}$

$t_{SYS}=1/f_{SYS}$

4-wire Serial Interface

Command Format

Software setups are used to configure the device. There are two mode commands to configure the device resources and to transfer the LED display data. The configurations are setup using the command mode which has a command mode ID of 100. The command mode consists of a system configuration command, a system frequency selection command, an LED configuration command and an operating command. The data mode includes READ, WRITE, and READ-MODIFY-WRITE operations.

The accompanying table shows the data and command mode IDs.

Operation	Mode	ID
Read	Data	110
Write	Data	101
Read-Modify-Write	Data	101
Command	Command	100

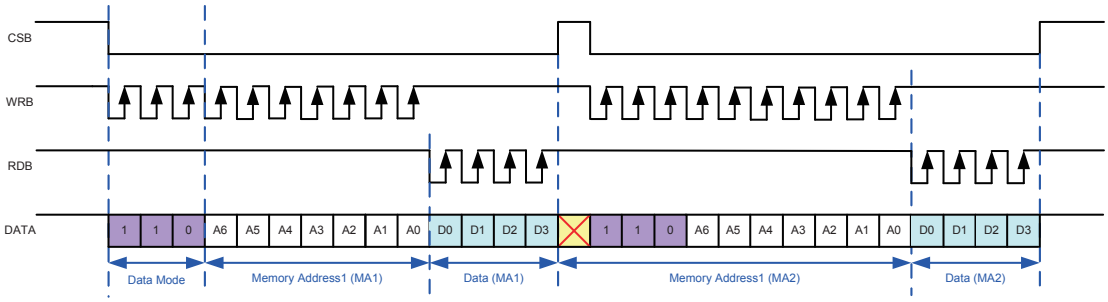
The mode command should be issued before any data or other commands are transferred. If successive commands have been issued, the command mode ID, namely 100, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the CSB pin should be set to "1" and the previous operation mode will be reset also. Once the CSB pin returns to "0", a new operation mode ID should be issued first.

Interfacing

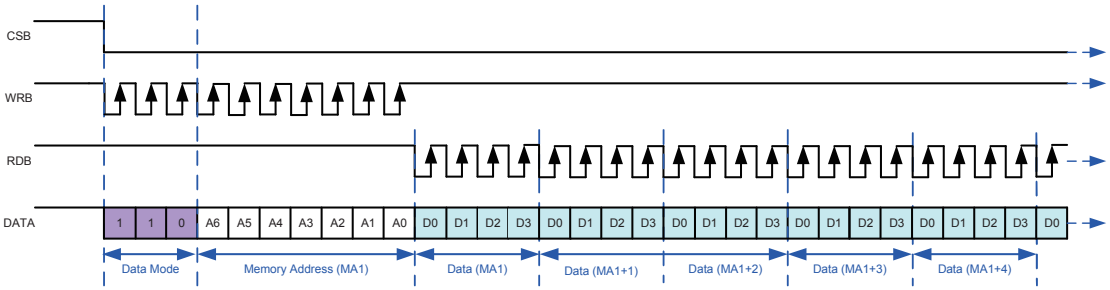
Only four lines are required to interface to the device. The CSB line is used to initialise the serial interface circuit and to terminate the communication between the host controller and the device. If the CSB pin is set high, the data and command issued between the host controller and the device are first disabled and then initialised. Before issuing a mode command or before mode switching, a high level pulse is required to initialise the device serial interface. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be transferred on the DATA line. The RDB line is the READ clock input. Data in the RAM is clocked out on the falling edge of the RDB signal and will appear on the DATA line. It is recommended that the host controller read in the correct data during the interval between the rising edge and the next falling edge of the RDB signal. The WRB line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the device on the rising edge of the WRB signal.

4-Wire Timing Diagram

Read Mode − Command Code = 110

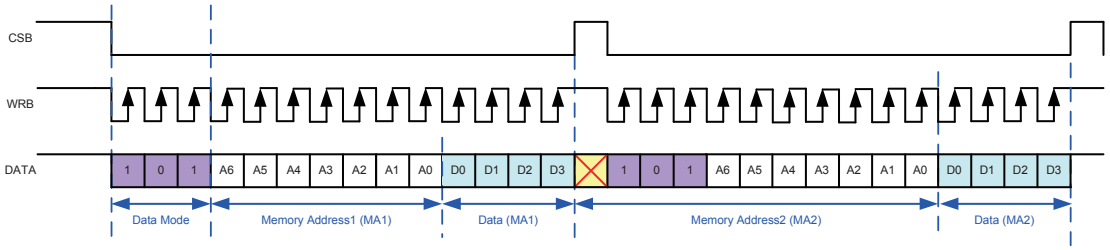


Read Mode − Successive Address Reading

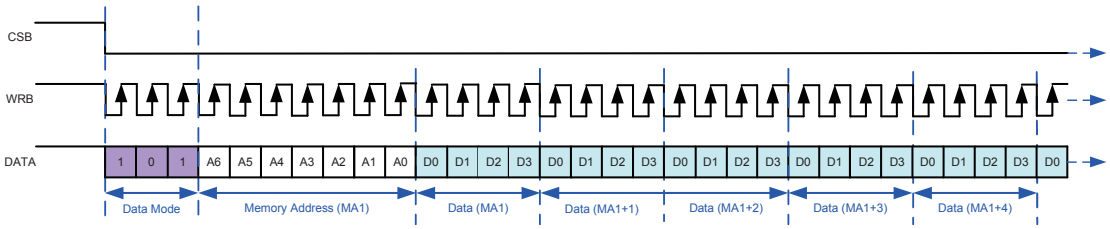


Note: After reaching the display memory location 0X57H the pointer will reset to 0X00H.

Write Mode − Command Code = 101

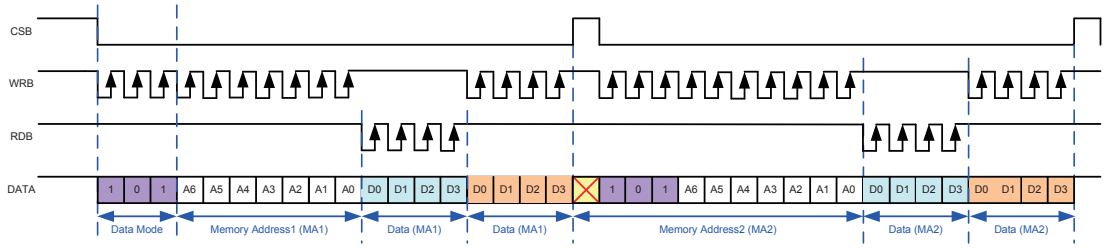


Write Mode − Successive Address Writing

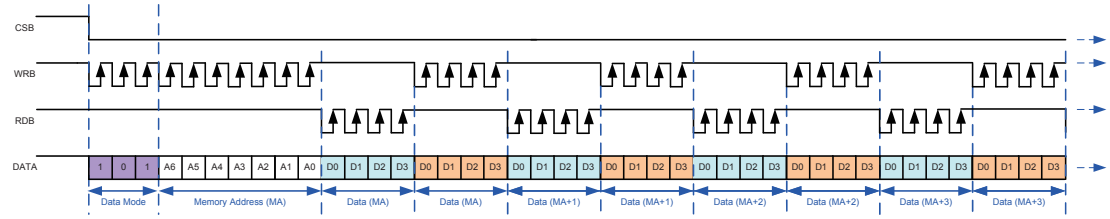


Note: After reaching the display memory location 0X57H the pointer will reset to 0X00H.

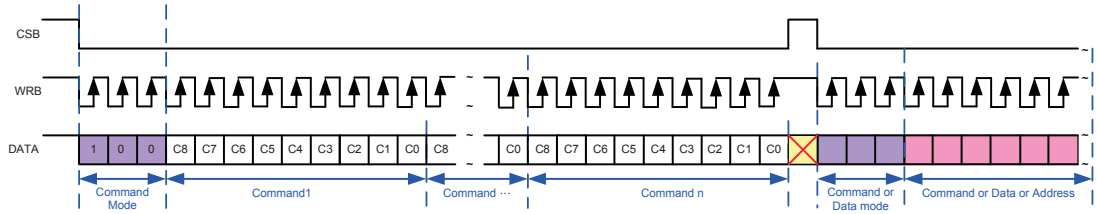
Read-Modify-Write Mode − Command Code = 101



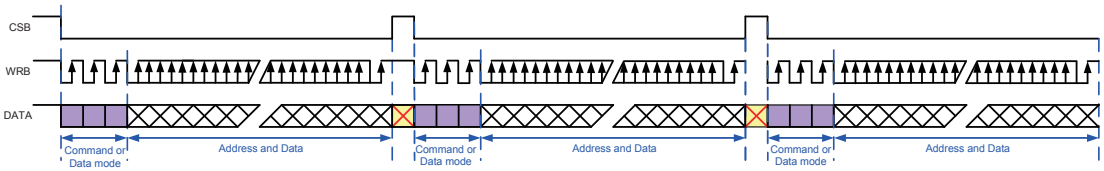
Read-Modify-Write Mode − Successive Address Accessing



Command Mode − Command Code = 100



Mode − Data and Command Mode



4-wire Serial Bus Command Summary

Name	ID	Command code	D/C	Function	Def.
Read	110	A6A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
Write	101	A6A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
Read-Modify-Write	101	A6A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator and LED duty cycle generator	Yes
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LED OFF	100	0000-0010-X	C	Turn off LED duty cycle generator	Yes
LED ON	100	0000-0011-X	C	Turn on LED duty cycle generator	
Blink OFF	100	0000-1000-X	C	Turn off blinking function	Yes
Blink_ON_2Hz	100	0000-1001-X	C	Turn on 2Hz blinking function	
Blink_ON_1Hz	100	0000-1010-X	C	Turn on 1Hz blinking function	
Blink_ON_0.5Hz	100	0000-1011-X	C	Turn on 0.5Hz blinking function	
Slave Mode	100	0001-0XXX-X	C	• Slave mode • Clock source from external clock • System clock input is on the OSC pin • Synchronous signal input is on the SYNC pin	
RC Master Mode0	100	0001-100X-X	C	• Master mode • Clock source from on-chip RC oscillator • OSC pin remains low • SYNC pin remains high • Single chip application only	Yes
RC Master Mode1	100	0001-101X-X	C	• Master mode • Clock source from on-chip RC oscillator • System clock output on the OSC pin • Synchronous signal output on the SYNC pin	
EXT CLK Master Mode0	100	0001-110X-X	C	• Master mode • Clock source from external clock, • System clock input on the OSC pin • SYNC pin remains high • Single chip application only	
EXT CLK MASTER MODE1	100	0001-111X-X	C	• Master mode • Clock source from external clock • System clock input on the OSC pin • Synchronous signal output on the SYNC pin	

Note: It is not recommended to change between MASTER and SLAVE mode after system enable (SYS_EN=1).

Name	ID	Command code	D/C	Function	Def.
COM OPTION	100	0010-aXXX-X	C	Bit “a” : Open drain type selection a=0: N-MOS a=1: P-MOS	a=0
PWM Duty	100	101X-0000-X	C	PWM 1/16 Duty	
	100	101X-0001-X	C	PWM 2/16 Duty	
	100	101X-0010-X	C	PWM 3/16 Duty	
	100	101X-0011-X	C	PWM 4/16 Duty	
	100	101X-0100-X	C	PWM 5/16 Duty	
	100	101X-0101-X	C	PWM 6/16 Duty	
	100	101X-0110-X	C	PWM 7/16 Duty	
	100	101X-0111-X	C	PWM 8/16 Duty	
	100	101X-1000-X	C	PWM 9/16 Duty	
	100	101X-1001-X	C	PWM 10/16 Duty	
	100	101X-1010-X	C	PWM 11/16 Duty	
	100	101X-1011-X	C	PWM 12/16 Duty	
	100	101X-1100-X	C	PWM 13/16 Duty	
	100	101X-1101-X	C	PWM 14/16 Duty	
	100	101X-1110-X	C	PWM 15/16 Duty	
	100	101X-1111-X	C	PWM 16/16 Duty	Yes

Note: 1. X: Don’t care

2. A7~A0: RAM addresses

3. D3~D0: RAM data

4. D/C: Data/command mode

5.Def.: Power on reset default

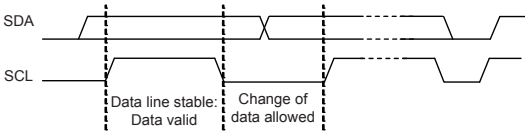
6. All the bold forms, namely 110, 101, and 100, are mode commands. Among these, 100 indicates the command mode ID. If successive commands have been issued, the command mode ID except for the first command will be omitted. The source of the tone frequency and of the time base clock frequency can be derived from an on-chip RC oscillator or an external clock. Calculation of the frequency is based on the system frequency sources as stated above. It is recommended that the host controller should initialise the device after a power on reset, as if the power on reset fails, this will lead to device malfunction.

I²C Serial Interface

The device includes an I²C serial interface. The I²C bus is a bidirectional, two-line communication link between different ICs or modules. The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to a positive supply via a pull-up resistor, typical 10kΩ for 100kHz. When the bus is free both lines are high. The output stages of devices connected to the bus must have open-drain or open-collector types in order to implement a wired and function. Data transfer is initiated only when the bus is not busy.

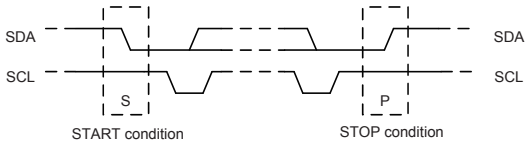
Data Validity

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low as shown in the accompanying diagram.



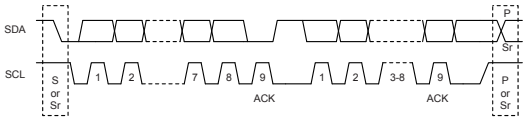
START And STOP Conditions

- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus stays busy if a repeated START(Sr) is generated instead of a STOP condition. The START(S) and repeated START(Sr) conditions are functionally identical.



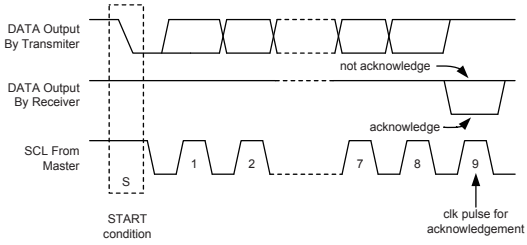
Byte Format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.



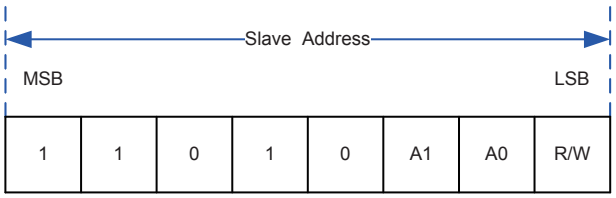
Acknowledge

- Each byte of eight bit length is followed by one acknowledge bit. This acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse.
- A slave receiver which is addressed must generate an acknowledge, ACK, after the reception of each byte.
- The device that provides an acknowledge must pull down the SDA line during the acknowledge clock pulse so that it remains at a stable low level during the high period of this clock pulse.
- A master receiver must signal an end of data to the slave by generating a not-acknowledge, NACK, bit on the last byte that has been clocked out of the slave. In this case, the master receiver must leave the data line high during the 9th pulse so as to not acknowledge. The master will generate a STOP or a repeated START condition.



Slave Addressing

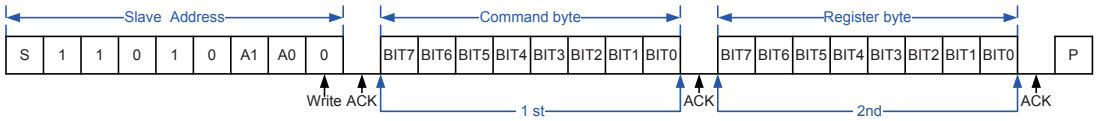
- The device requires an 8-bit slave address word following a start condition to enable the chip for a write operation. The device address words consist of a mandatory one, zero sequence for the first four most significant bits. Refer to the diagram showing the slave Address. This is common to all LED devices.
- The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines whether a read or write operation is to be performed. When the R/W bit is “1”, then a read operation is selected. A “0” selects a write operation.
- The address bits are “1, 1, 0, 1, 0, A1, A0”. When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.



I²C Timing Diagram

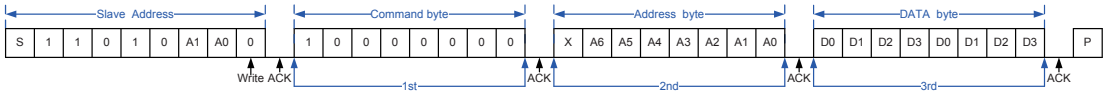
Write Operation – Command Byte

Byte write operation requires a START condition, slave address with R/W bit, a command (1st), a register byte command (2nd) and a STOP condition for the command byte.



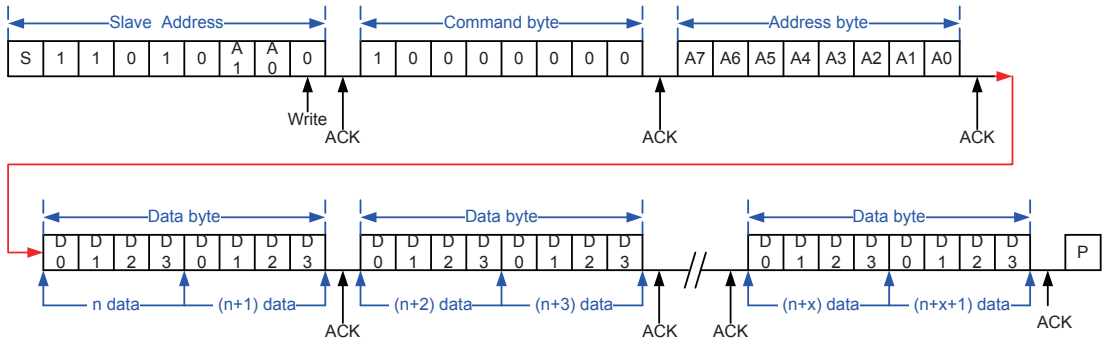
Write Operation – Write Display RAM Single Data Byte

A display RAM data byte write operation requires a START condition, a slave address with a write control bit, a valid display data input /output command, Address byte, a Data byte and a STOP condition.

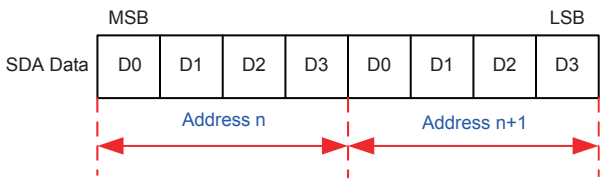


Write Operation – Page Write Display Data Operation

Following a START condition, the slave address together with the R/W bit is placed on the bus. The addressed device will then be provided with an address, which is the address pointer where the data is to be written. The data to be written then follows after which the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. After reaching the display memory location 0X57H the pointer will reset to 0X00H



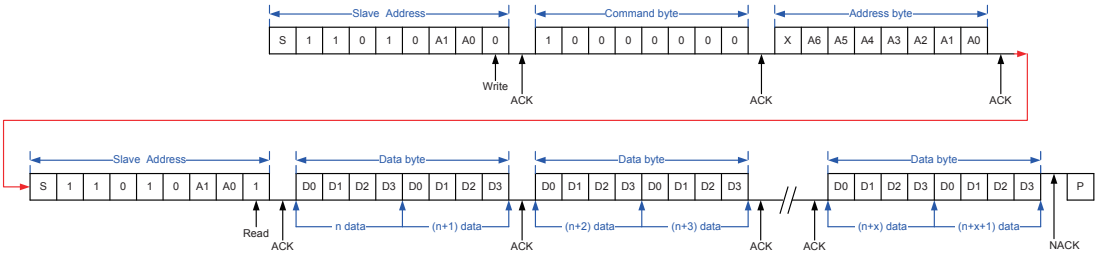
Note: The relationship between the LCD Display Input/ Output Data transfer format and the RAM mapping data format is shown below.



Read Operation – Read Display Data Operation

In this mode, the master reads the device data after setting the slave address. Following the R/W bit, which is zero, and the acknowledge bit, then follows the display data address setting command code (1st). After this is the address pointer (An) which is written to the address pointer (2nd). Next comes the START condition and slave address, followed by an R/W bit which is high. The data which was addressed is then transmitted. The address pointer is only incremented on reception of an acknowledge clock. The device will place the data at address An+1 onto the bus. The master reads and acknowledges the new byte and the address pointer is incremented to "An+2".

- If the memory location exceeds the limit value of 0X57H, the memory pointer will return to 00H.
- If only a read command is sent to the I²C interface, then dummy data is sent out.
- This cycle for reading consecutive addresses will continue until the master sends a NACK and STOP condition.
- Read display data format



I²C Bus Command Summary

Display Data Input Command

This command sends data from the MCU to the device memory map.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Display Data Input/ output command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	A6	A5	A4	A3	A2	A1	A0	Displays data start address of the memory map	W	00H

Note:
- Power on status: the address is set to 00H.
- If the programmed command is not defined the function will not be affected.

System Mode Command

This command controls the system oscillator on/off and display on/off.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
System mode setting command	1st	1	0	0	0	0	0	1	0		W	
System oscillator and display on/off setting	2nd	X	X	X	X	X	X	P1	P0		W	00H

Note:

Name	Bit		System Oscillator	LED Display
	P1	P0		
SYS DIS and LED off	0	X	Off	Off
SYS EN and LED off	1	0	On	Off
SYS EN and LED on	1	1	On	On

- Power on status: Display off and disable the internal system oscillator.
- If the programmed command is not defined, the function will not be affected.

Blinking Frequency Command

This command defines the blinking frequency of the display modes.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Blinking frequency command	1st	1	0	0	0	0	1	0	0		W	
Blinking frequency setting	2nd	X	X	X	X	X	X	P1	P0		W	00H

Note:

Bit		Blinking Frequency
P1	P0	
0	0	Blinking off
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

- Power on status: Blinking function is switched off.
- If the programmed command is not defined, the function will not be affected.

COM Option Command

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Driver output of COM setting command	1st	1	0	0	0	1	0	0	0		W	
COM pin option setting	2nd	X	X	X	X	X	X	X	P0		W	00H

Note:

Bit	COM pin open drain type selection
P0	
0	N-MOS
1	P-MOS

- Power on status: The COM N-MOS open drain output is setup.
- If the programmed command is not defined the function will not be affected.

Cascade Set Mode Command

This command will select master/slave mode and input clock source.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
Cascade set mode command	1st	1	0	1	0	0	0	0	0		W	
Master/ slave select and input clock source setting	2nd	X	X	X	X	X	P2	P1	P0		W	04H

Note:

Name	Bit			Master/Slave Select	Input Clock Source	OSC pin Status	Sync pin Status	Note
	P2	P1	P0					
RC Master Mode0	1	0	0	Master mode	On Chip RC Oscillator	Output Hi-Z	Always Output high	Only single chip application
RC Master Mode1	1	0	1			Output	Output	
EXT CLK Master Mode0	1	1	0	Master mode	External OSC	Input	Always Output high	Only single chip application
EXT CLK Master Mode1	1	1	1			Input	Output	
Slave Mode	0	X	X	Slave mode	External OSC	Input	Input	

- Power on status: The RC MASTER MODE0 is selected.
- It is not recommended to change between MASTER and SLAVE mode after a system enable (SYS_EN=1)
- If the programmed command is not defined the function will not be affected.

PWM Duty Command

This command controls the row pulse width.

Function	Byte	(MSB) Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB) Bit0	Note	R/W	Def
System mode setting command	1st	1	1	0	0	0	0	0	0		W	
System oscillator and display on/off setting	2nd	X	X	X	X	P3	P2	P1	P0		W	0FH

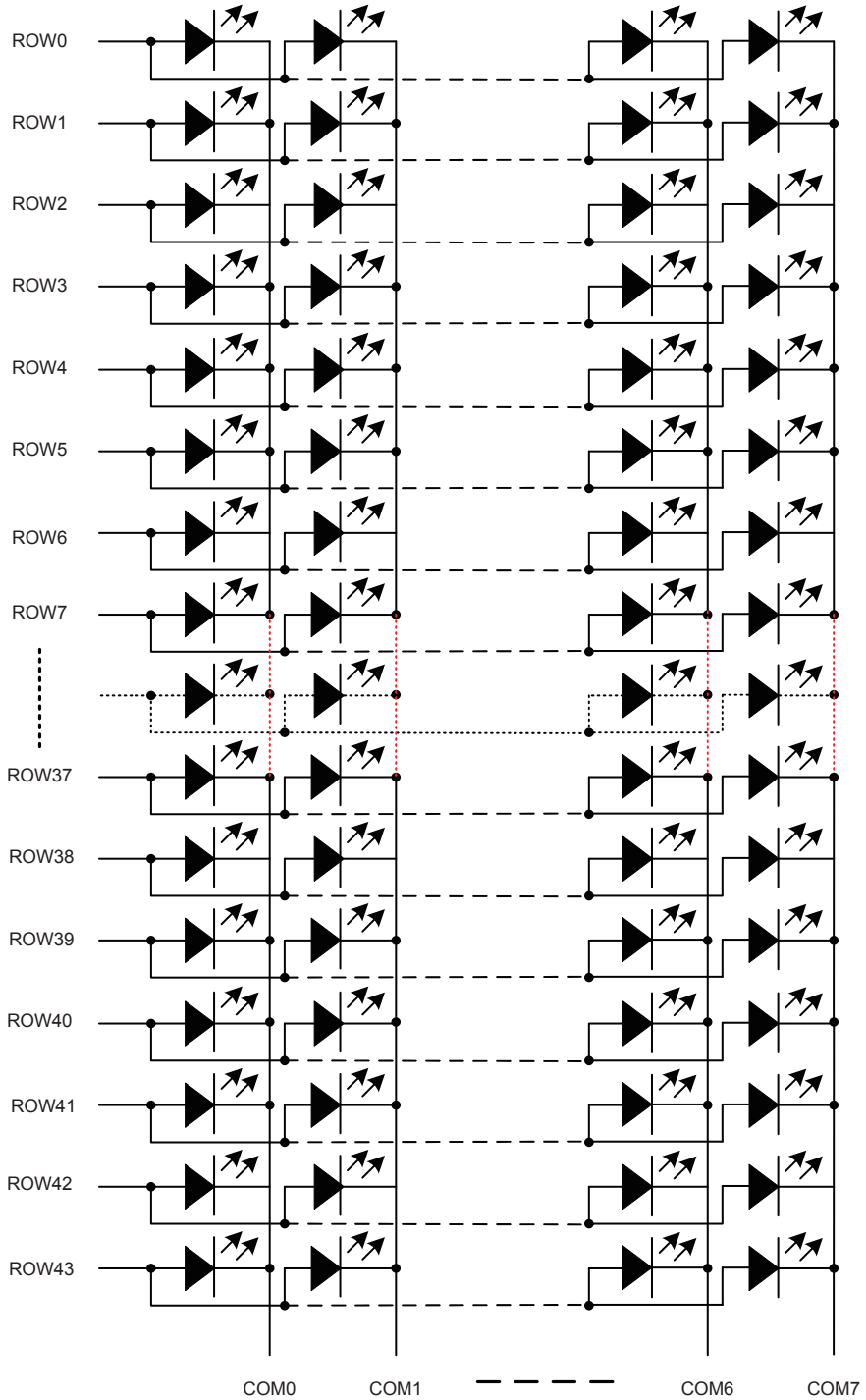
Note:

Bit				PWM duty
P3	P2	P1	P0	
0	0	0	0	1/16
0	0	0	1	2/16
0	0	1	0	3/16
0	0	1	1	4/16
0	1	0	0	5/16
0	1	0	1	6/16
0	1	1	0	7/16
0	1	1	1	8/16
1	0	0	0	9/16
1	0	0	1	10/16
1	0	1	0	11/16
1	0	1	1	12/16
1	1	0	0	13/16
1	1	0	1	14/16
1	1	1	0	15/16
1	1	1	1	16/16

- Power on status: 16/16 PWM duty is selected.
- If the programmed command is not defined the function will not be affected.

Application Circuits

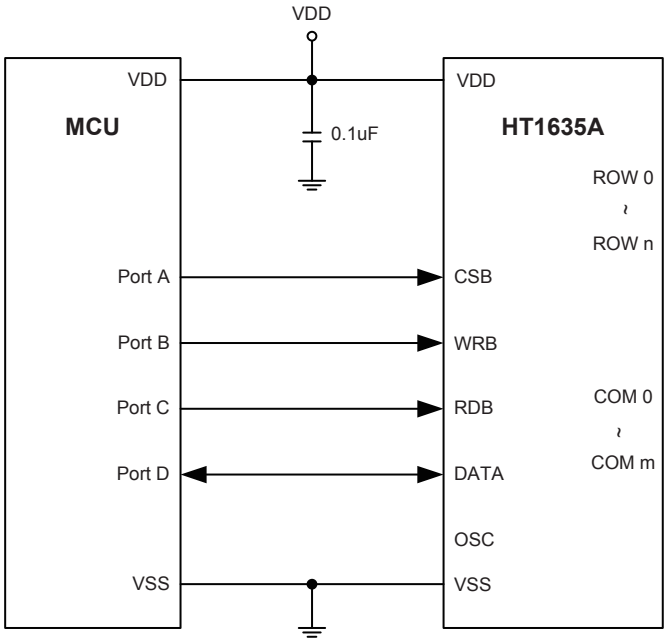
LED Matrix Circuit



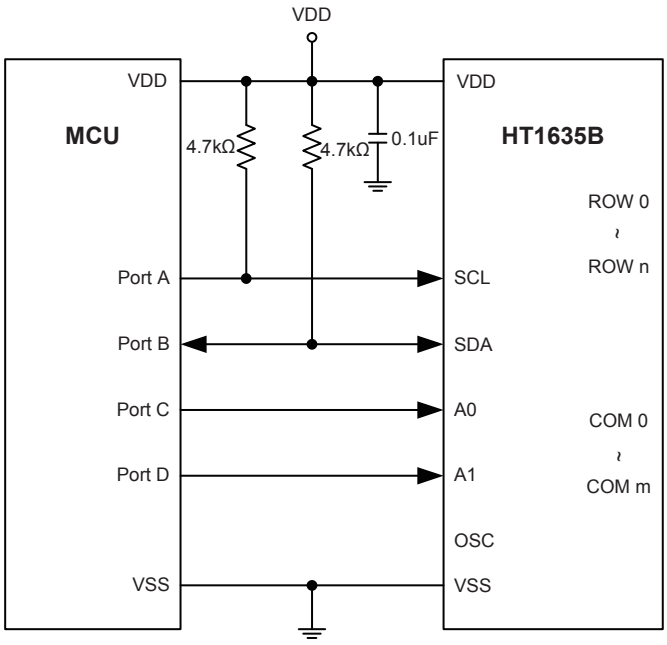
LED Display -- 44 ROW × 8 COM

Communication Bus Type Circuit

The device is compatible with most microcontrollers and communicates using two serial interfaces, an I²C bus or a 4-wire serial bus.



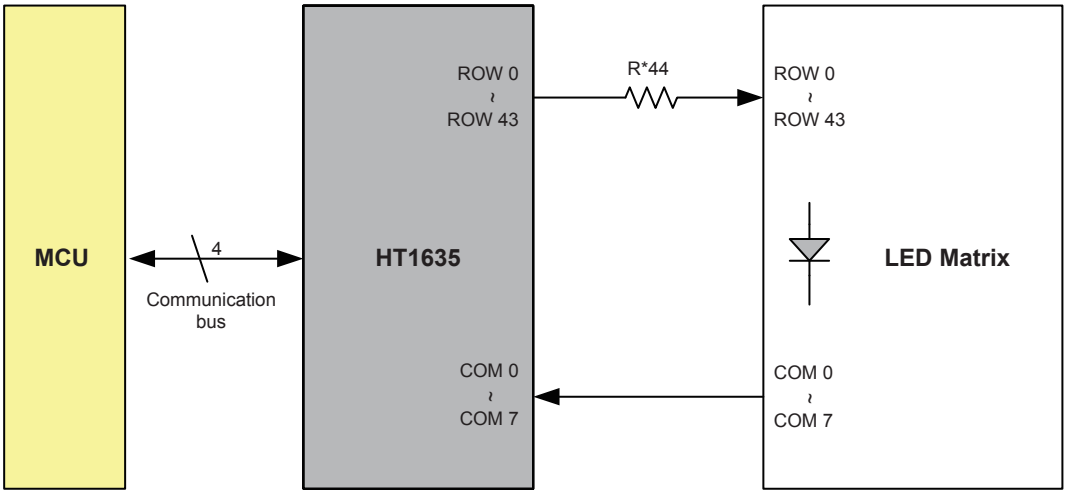
4-Wire Serial Bus



I²C Serial Bus

Low Power LED Application – Direct Drive

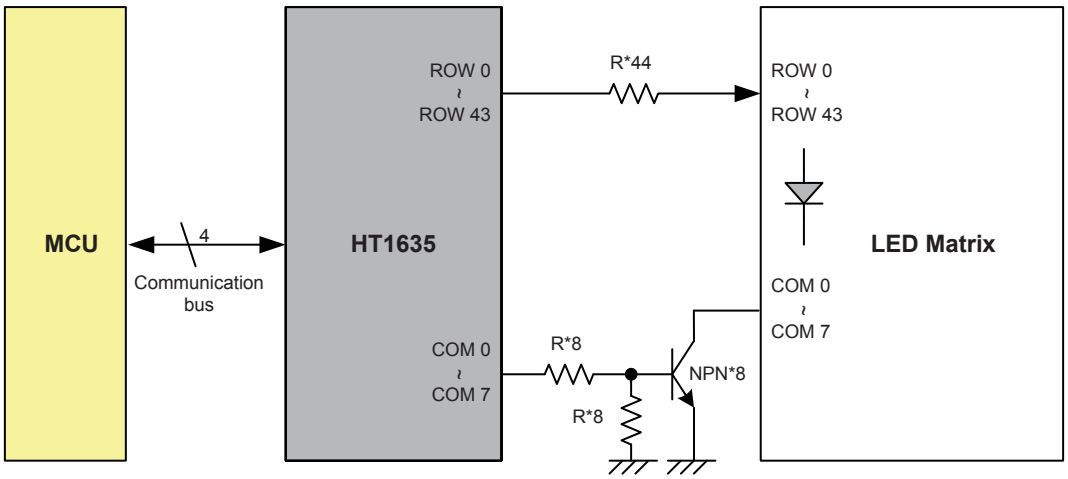
44 ROW × 8 COM Example: N-MOS Open Drain Output



Note: Values of the R resistors are selected depending on the power consumption of the LEDs.

Middle Power LED Application – COM with Transistor Buffer

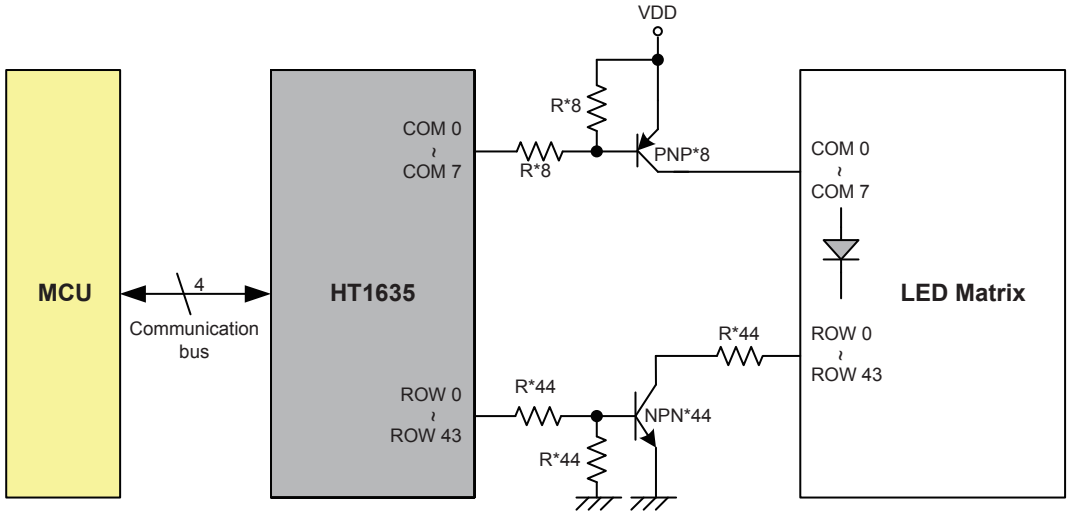
44 ROW × 8 COM Example – P-MOS Open Drain Output and 8 COM Option



Note: Values of the R resistors are selected depending on the power consumption of the LEDs.

High Power LED Application – ROW & COM with Transistor Buffer

44 ROW × 8 COM Example – N-MOS Open Drain Output

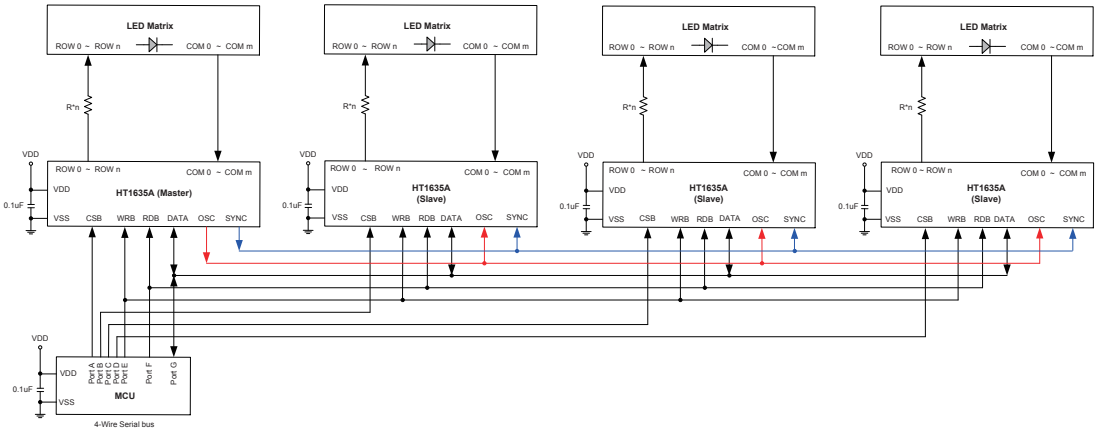


Note: Values of the R resistors are selected depending on the power consumption of the LEDs.

Cascade Function

Low Power LED Application

- **Example: Direct Driving for 4-wire Serial Bus**

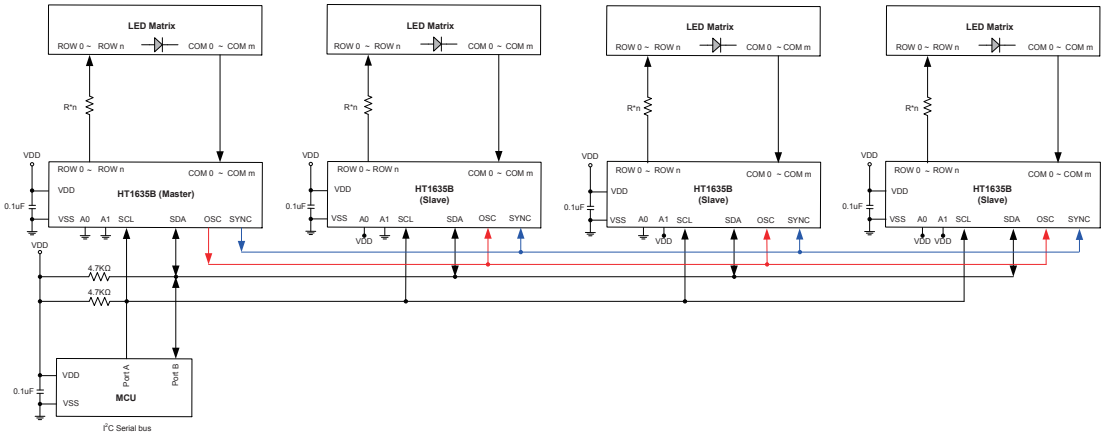


Note: 1. Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using the commands. The CSB pin must be connected to the uC individually for independent read and write.

2. Values of the R resistors are selected depending on the power consumption of the LEDs.

3. When the COM option selects N-MOS open drain outputs then m=7, n=43.

- **Example: Direct Driving for I²C Serial Bus**



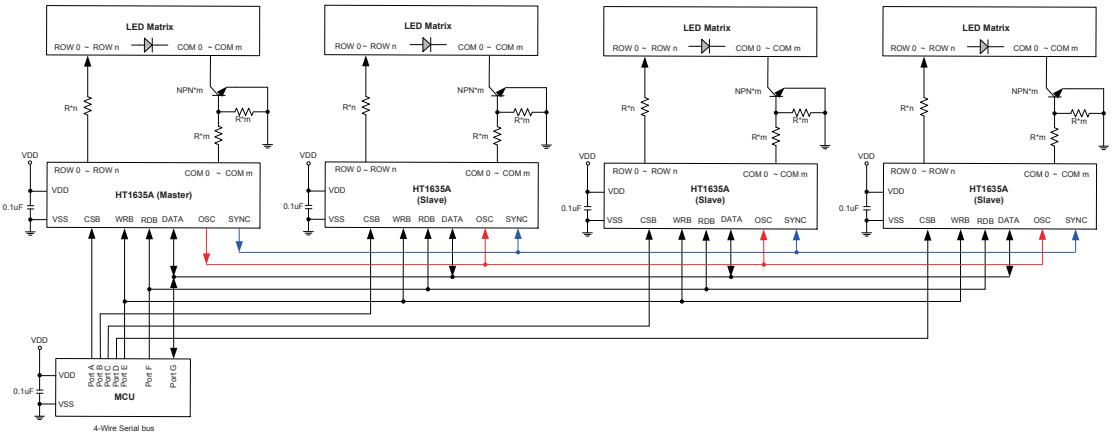
Note: 1.Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using the commands. The CSB pin must be connected to the uC individually for independent read and write.

2. Values of the R resistors are selected depending on the power consumption of the LEDs.

3. When the COM option selects N-MOS open drain outputs then m=7, n=43.

Medium Power LED Application

- **Example: COM with Transistor Buffer for 4-wire Serial Bus**

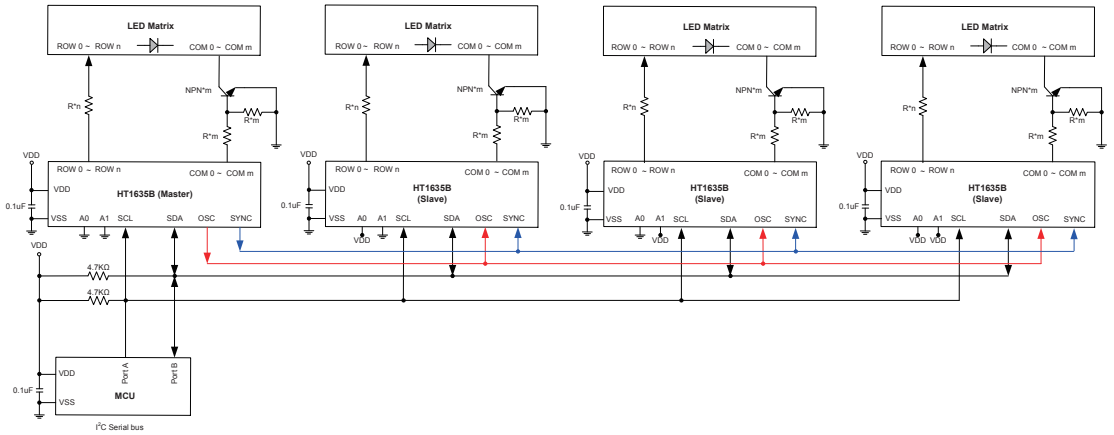


Note: 1. Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using the commands. The CSB pin must be connected to the uC individually for independent read and write.

2. Values of the R resistors are selected depending on the power consumption of the LEDs.

3. When the COM option selects N-MOS open drain outputs then m=7, n=43.

- **Example: COM with Transistor Buffer for I²C Serial Bus**



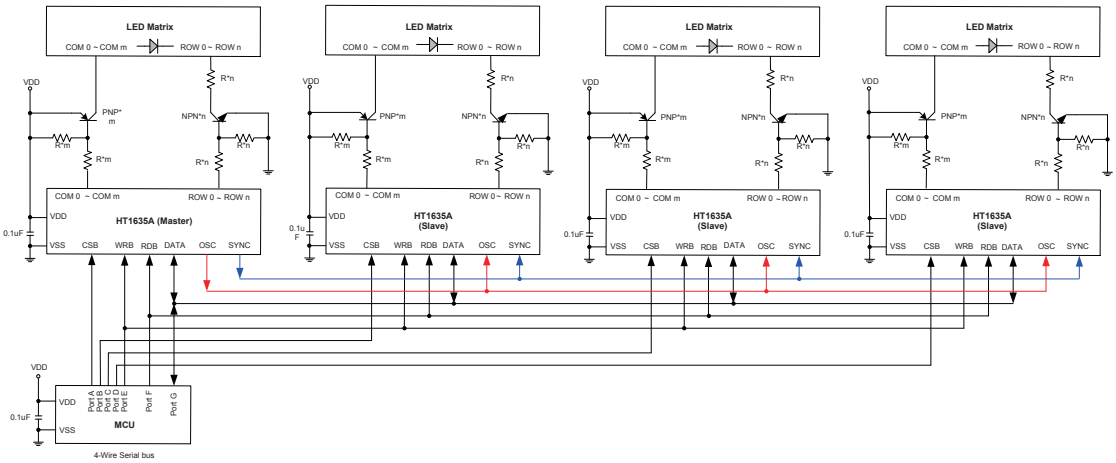
Note: 1. Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using the commands. The CSB pin must be connected to the uC individually for independent read and write.

2. Values of the R resistors are selected depending on the power consumption of the LEDs.

3. When the COM option selects N-MOS open drain outputs then m=7, n=43.

High Power LED Application – ROW & COM with Transistor Buffer

- **Example: ROW & COM with Transistor Buffer for 4-wire Serial Bus**

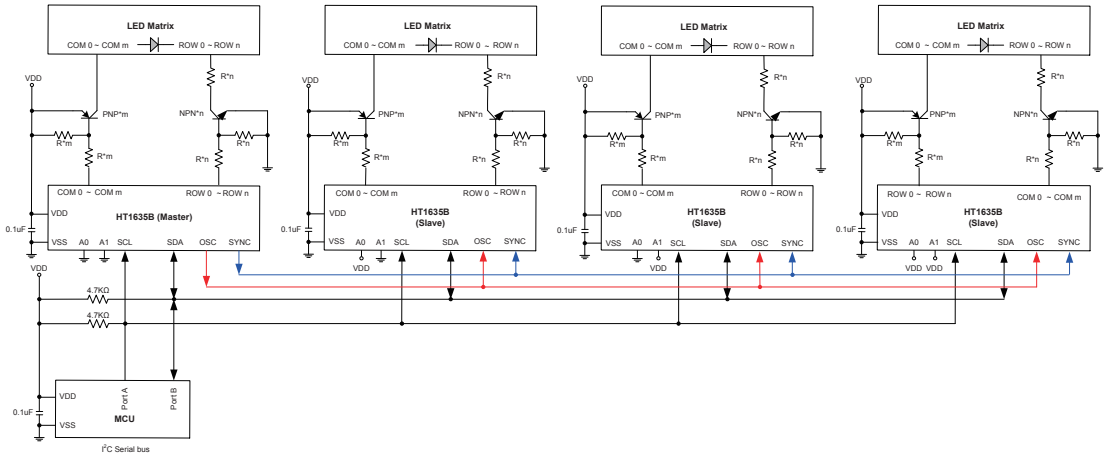


Note: 1. Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using the commands. The CSB pin must be connected to the uC individually for independent read and write.

2. Values of the R resistors are selected depending on the power consumption of the LEDs.

3. When the COM option selects N-MOS open drain outputs then m=7, n=43.

- **Example: ROW & COM with Transistor Buffer for I²C Serial Bus**

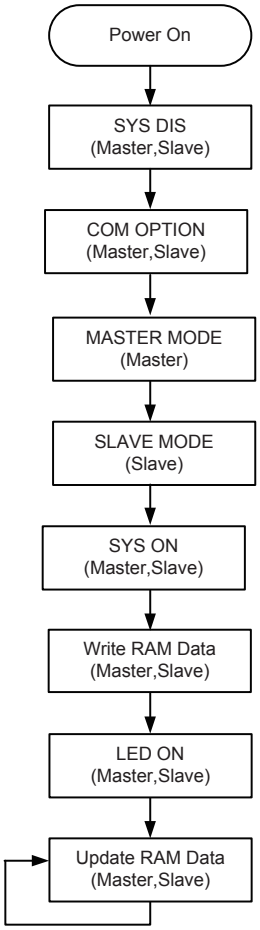


Note: 1. Cascading can also be implemented using software. Users must set the Master in the master mode and the Slave in the slave mode using the commands. The CSB pin must be connected to the uC individually for independent read and write.

2. Values of the R resistors are selected depending on the power consumption of the LEDs.

3. When the COM option selects N-MOS open drain outputs then m=7, n=43.

Cascade Control Flow



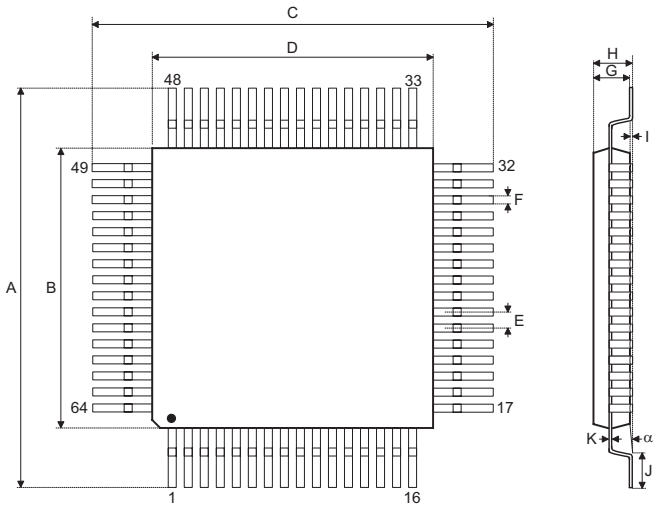
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the package information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Further Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

64-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.354 BSC	—
B	—	0.276 BSC	—
C	—	0.354 BSC	—
D	—	0.276 BSC	—
E	—	0.016 BSC	—
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	9.00 BSC	—
B	—	7.00 BSC	—
C	—	9.00 BSC	—
D	—	7.00 BSC	—
E	—	0.40 BSC	—
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°