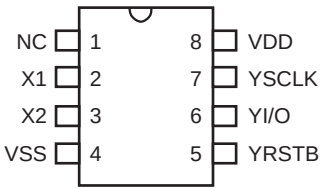
Features

* Full operation voltage from 2.0V to 5.5V
* Consumes less than 400nA at VDD=2V in operation
* Consumes less than 100nA at VDD=2V in standby condition
* Input serial clock (YSCLK) rate up to 500kHz at VDD=2V,2MHz at VDD=5V
* Real-time clock(RTC) counts seconds, minutes. hours, date of the month, month, day of the week, and year with leap-year compensation valid up to 2100.
* Three-wire serial I/O interface
* Two types of data transmission: single byte mode and burst mode
* Schmitt Trigger Input (window size, 2.2V~1.2V, @VDD=5V)
* SHT1302: 8 pins DIP SHT1302S: 8 pins SOP

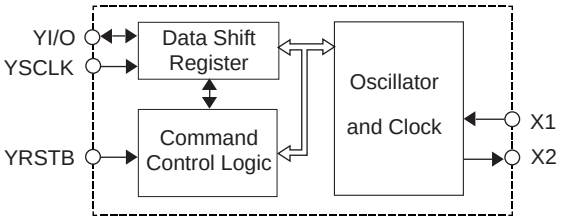
General Description

The SHT1302 is a 3-wire serial timekeeper chip, which contains mainly an RTC/Calendar function. It can be communicated with a microprocessor easily through a simple 3-wire interface. They are (1) YRSTB, (2) YSCLK and (3) YI/O. Data can be accessed with 1 byte at a time or up to 8 bytes in the burst mode. The SHT1302 provides seconds, minutes, hours, day, and date, month, and year information. The end of date is automatically adjusted for each month when it is needed and even in the leap year. Besides, the clock of the chip can operate in either the 12-hour or 24-hour format with an AM/PM indicator. An external 32768Hz crystal is also required to provide the chip a correct internal timing processing.

Pin Assignment



Blcok Diagram



Pin Description

Pad No.	Pin Name	I/O	Description
1	NC	-	Not connected
2.3	X1,X2	I	Off-chip 32.768kHz crystal
4	VSS	I	Ground pin
5	YRSTB	I	The reset pin of serial transmission
6	YI/O	I/O	The data input/output pin of serial transmission
7	YSCLK	I	The serial clock pulses pin of serial transmission
8	VDD	I	Power supply pin

Absolute Maximum Ratings

Supply Voltage.....-0.3V to 5.5V
Input Voltage.....Vss-0.3V to VDD+0.3V
Storage Temperature.....-50℃ to 125℃
Operating Temperature.....-40℃ to 85℃

D.C.Characteristics

(Ta=25°C)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operation voltage	—	—	2	—	5.5	V
I_{STB}	Stand-by current	2V	—	—	—	100	nA
		5V		—	—	100	nA
I_{DD}	Operation current	2V	No load	—	—	0.3	μA
		5V		—	—	1.0	mA
I_{OH}	Source current	2V	V_{OH}=1.8V	-0.2	-0.4	—	mA
		5V	V_{OH}=4.5V	-0.5	-1.0	—	mA
I_{OL}	Sink current	2V	V_{OL}=0.2V	0.7	1.5	—	mA
		5V	V_{OL}=0.5V	2.0	4.0	—	mA
V_{IH}	“H” iinput voltage	5V	—	2	—	—	V
V_{IL}	“L” input voltage	5V	—	—	—	0.8	V
F_{OSC}	System frequency	5V	32.768KHz XTAL	—	32.768	—	KHz
F_{SCLK}	Serial clock	2V	—	—	—	0.5	MHz
		5V		—	—	2	MHz

*I_{STB} is specified with SCLK, I/O, $\overline{RST}$ open. The clock halt bit must be set to logic one (oscillator disabled).

A.C.Characteristics

(Ta=25°C)

Symbol	Parameter	VDD	Min.	Max.	Unit
t_{DC}	Data to clock setup	2V	200	—	ns
		5V	50	—	
t_{CDH}	Clock to data hold	2V	280	—	ns
		5V	70	—	
t_{CDD}	Clock to data delay	2V	—	800	ns
		5V	—	200	
t_{CL}	Clock low time	2V	1000	—	ns
		5V	250	—	
t_{CH}	Clock high time	2V	1000	—	ns
		5V	250	—	
f_{CLK}	Clock frequency	2V	—	0.5	MHz
		5V	D.C.	2.0	
t_R t_F	Clock rise & fall time	2V	—	2000	ns
		5V	—	500	
t_{CC}	Reset to clock setup	2V	4	—	us
		5V	1	—	
t_{CCH}	Clock to reset hold	2V	240	—	ns
		5V	60	—	
t_{CWH}	Reset inactive time	2V	4	—	us
		5V	1	—	
t_{CDZ}	Reset to I/O high Z	2V	—	280	ns
		5V	—	70	

Function Description

The SHT1302 chip with accurate timekeeper function, it contains mainly three internal units. The first one is Oscillator and Clock unit, which combined with an external 32768Hz crystal to synchronize the internal clock. The second is Command and Control unit, which is used to decode the different input commands and output a series of correct control signal, and the last unit is Data Shift Register which converts the serial input data to parallel out, and then processed by control unit, or converts parallel input data, after processed to serial out taken as a primary output data.

The SHT1302 chip also contains two additional bits, the clock halt bit (CH), and the write protect bit (WP). The CH bit decides the internal clock signal to operate or not, and the WP bit decides whether the internal registers can be written into or not. Both of these two bits should be specified first before chip can function properly.

Command byte

Each data transfer is initiated by a command byte setting. The table shown below illustrates the different function chosen by different contents of command byte. The least bit "C0" determines a read or write cycle to be performed, and bits C3~C1 denoted as A2~A0, are use to specify one of eight registers can be accessed. Besides, the burst mode is selected when the code BE (or BF) of command byte is written into the chip. In addition, after command byte code 8E is set, the next written data bit 7 should be set to "0" to release the write protection. Similarly, in order to turn on the clock, the following written data bit 7 also should be set to "0" after command byte code 80 has been written into the chip. The command byte is shown as follows:

7	6	5	4	3	2	1	0
1	0	0	A3	A2	A1	A0	R/$\overline{W}$
				C3	C2	C1	C0

A0~A2 : The address of register.
A3 : 1 for test mode, 0 for normal mode.
R/$\overline{W}$: 1 for read cycle, 0 for write cycle.

The following table shows the register address and its data format:

Register address A2~A0	Function	Command Address (HEX)	Write=W Read=R	Range Data (BCD)	Register Definition							
					7	6	5	4	3	2	1	0
0	Seconds	80 81	W R	00~59	CH	10 SEC			SEC			
1	Minutes	82 83	W R	00~59	0	10 MIN			MIN			
2	12HRS 24HRS	84 85	W R	01~12 00~23	12\ 24	0 0	AP 10	HR HR	HOUR			
3	Date	86 87	W R	01~31	0	0	10 DATE		DATE			
4	Month	88 89	W R	01~12	0	0	0	10M	MONTH			
5	Day	8A 8B	W R	01~07	0	0	0	0	DAY			
6	Year	8C 8D	W R	00~99	10 YEAR				YEAR			
7	Write Protect	8E 8F	W R	00~80	WP	ALWAYS ZERO						

CH : Clock Halt bit.
CH=0 oscillator enabled.
CH=1 oscillator disabled.

WP : Write Protect bit.
WP=0 register data can be written in.
WP=1 register data can not be written in.

Bit 7 of Reg2 : 12/24 mode flag.
bit 7=1, 12-hour mode.
bit 7=0, 24-hour mode.

Bit 5 of Reg2 : AM/PM mode defined.
AP=1 PM mode.
AP=0 AM mode.

Bit C0 ($\overline{R/W}$ mode)
The least bit of Command byte is defined as a flag, which used to determine the status of data registers. When bit C0 is set to "0", a write cycle is expected, and data can be written into registers. Otherwise, the chip stays in the read cycle, and data only can be read out from registers.

C3~C1 Bits (A_2~A_0 Bits)
Bits C3~C1 of Command byte is used to specify which register will be accessed. There are total 8 registers contained in the chip for controlling different time units, as shown in the table. Before writing data into these registers, the write cycle should be asserted using the bit C0 of command byte.

Burst mode
When the Command byte is set to BE (BF), the chip enters the burst mode. In this mode the 8 registers can be written (or read) sequentially starting with bit 0 of register 0. (Refer to the timing waveform of burst mode in the next page)

Test mode
When the Command byte is set to 1001xxx1, the chip is in the test mode. The test mode is only used by chip provider internally. It is not recommended to use this mode by user while in the normal operation.

Write protect register
By setting bit7 (WP) of this register to logic 1, the other 7 registers can be protected to avoid unintentional writing. Data can be written into these registers only if the value of bit WP is set to logic 0. The bit WP of Write protect register also should be set to logic 0 first before re-starting the chip or writing the new data. It should be set to logic 1 in the read cycle. Besides, the WP bit cannot be set during the burst mode.

Clock Halt bit
The bit D7 of the Second register is defined as a Clock Halt bit. When this bit is set to logic 1, the internal clock oscillator is halted and chip enters the standby mode. This internal clock oscillator will be awaken up after re-setting bit D7 to logic 0.

12-hour/24-hour mode
The 12-hour or 24-hour mode selection is chosen by bit D7 of the hour register. When bit D7 is set to logic 1, the mode 12-hour is selected, otherwise 24-hour mode is chosen.

AM-PM mode
There are two functions chosen by bit D5 of the Hour register and determined by bit D7 of the same register. One is used in AM-PM mode selection when 12-hour mode is asserted. When bit D5 is set to logic 1, it is in PM mode, otherwise it is in AM mode. The other function of bit D7 is use to represent the second 10-hour bit (20~23) when 24-hour mode is chosen. When D7 is set to logic 1, combined with bit D4, 20~24 hour can be counted.

Reset (YRSTB) and Serial clock control (YSCLK)
The YRSTB pin is used to clear contents of some of internal registers. It needed to be asserted, from low to high, to initiate the chip and remained to logic 1 when chip is in normal operation. Besides, The YRSTB pin should be toggled, from low to high, at beginning of each access cycle and high to low at end of each access cycle. The YRSTB pin is also used to terminate either single byte or burst mode.
The YSCLK pin is the input clock pin used to synchronize the read or write data. In the read cycle, the output data is available after the last falling edge of the YSCLK in which the Command cycle is finished. And the input data must be ready before the first input YSCLK rising edge either in the Command write cycle or the data write cycle. The detail waveforms of both read and write cycles are illustrated in the next page.

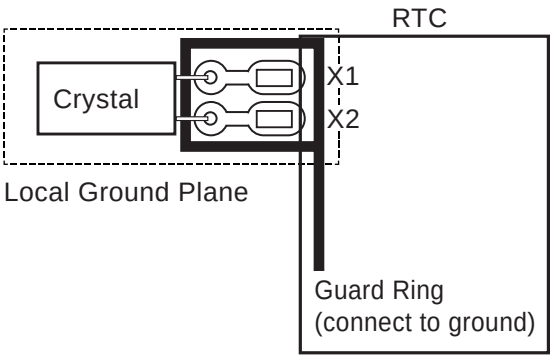
YI/O Signal
Pin YI/O is a bi-directional port used as the data writing into or data read from the chip. Before data writing into the chip, the bit R/$\overline{W}$ of the Command byte should be set to logic 0. Then data (Command byte or data) can be written into the chip following the first input clock signal YSCLK. Besides, data (Command byte or data) is written into the chip with the bit 0 firstly and

next 7 consecutively cycles. Additional YSCLK cycles will be ignored. Similarly, the bit R/$\overline{W}$ of the Command byte should be set to logic 1 before data can be read from the chip. The bit 0 is first read out at the falling edge of YSCLK and next 7 consecutively cycles, after the last bit of read Command byte is written into the chip. Except the total 8 YSCLK read cycle, the additional cycles will read data repeatedly as long as the YRSTB signal remains at the logic 1.

Crystal

A 32768Hz crystal can be directly connected to the SHT1302 chip via pin 2 and pin 3 (X1, X2). In order to obtain the corrent frequency, a crystal with two trimming capacitance, should be selected.

Recommended Layout For Crystal



Clock Accuracy

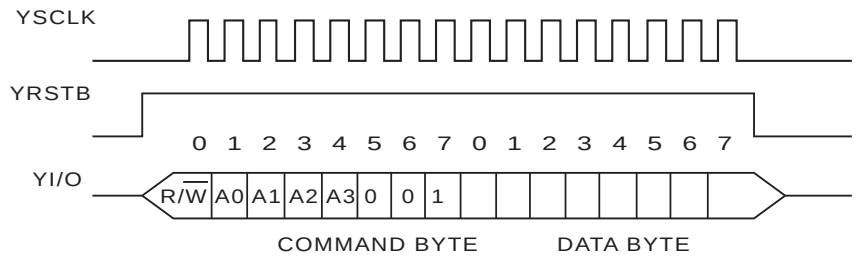
The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capactive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast.

Flowchart Representation

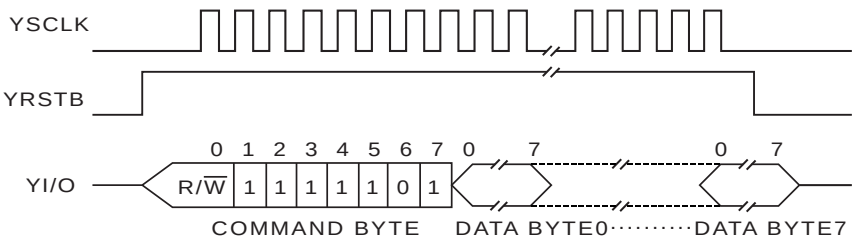
To initiate the chip, the write protect bit (WP) and internal oscillator enable bit (CH) should be released first after YRSTB input signal change from low to high. The WP bit is released by writing a Command byte 8E into chip, and followed by a data byte that MSB bit should be set to logic 0. Similarly, the bit CH is released by writing a Command byte 80 into chip, and followed by a data byte that MSB bit also should be set to logic 0. It must be noticed that there is a double transition of input signal YRSTB between bit WP and bit CH released. In other words, the signal YRSTB needed to be re-asserted between two consecutively access. After bit WP and CH are released, the chip is ready for accessed by external host (ex. Microprocessor). In the single byte mode, there are 16 YSCLK pulses needed to access data, or 72 pulses in the burst mode.

The following diagram shows the single and burst mode transfer:

Single Byte Transfer

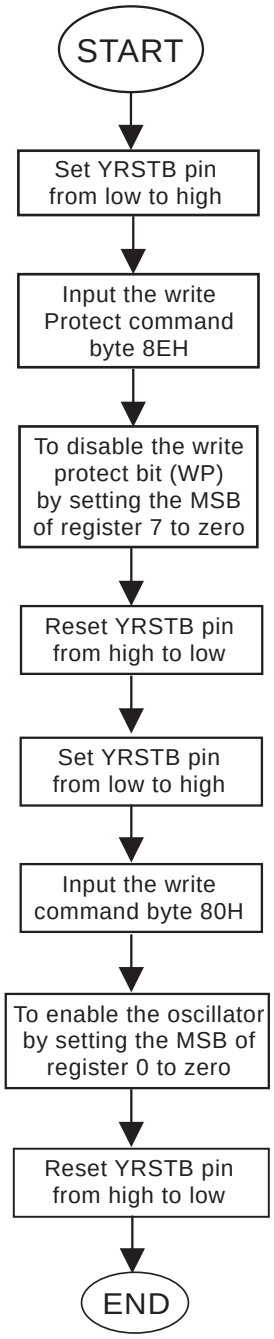


Burst Mode Transfer

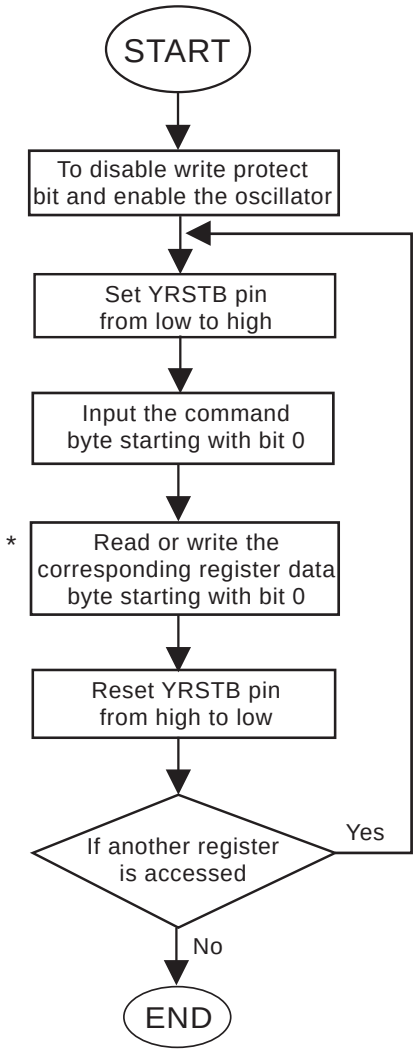


Flow Chart

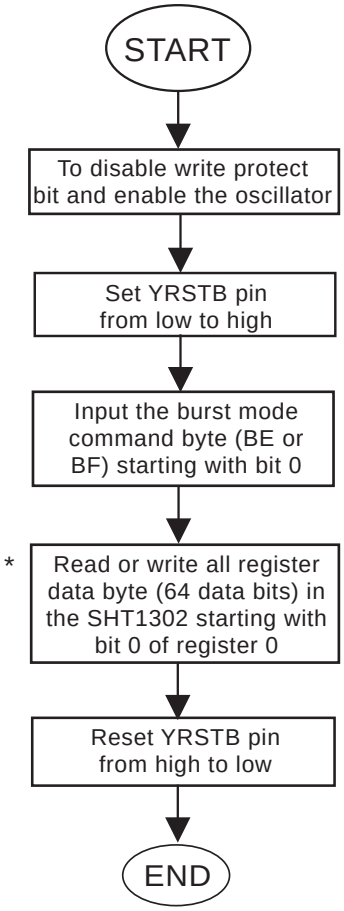
* To disable write protect (WP=0) bit and enable the oscillator (CH=0)



* Single byte data transfer



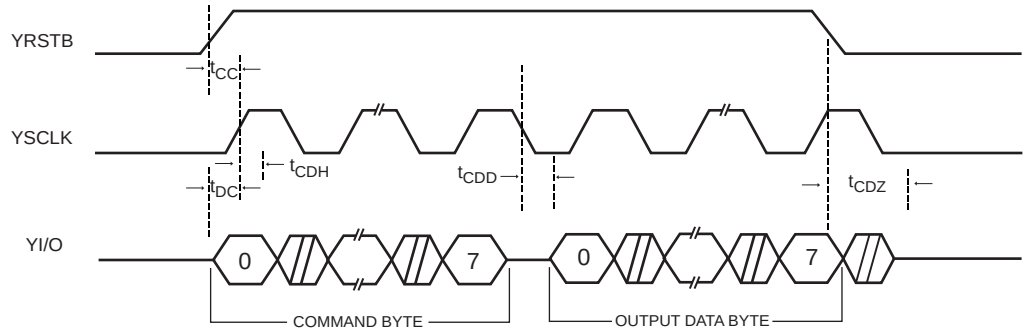
* Burst mode data transfer



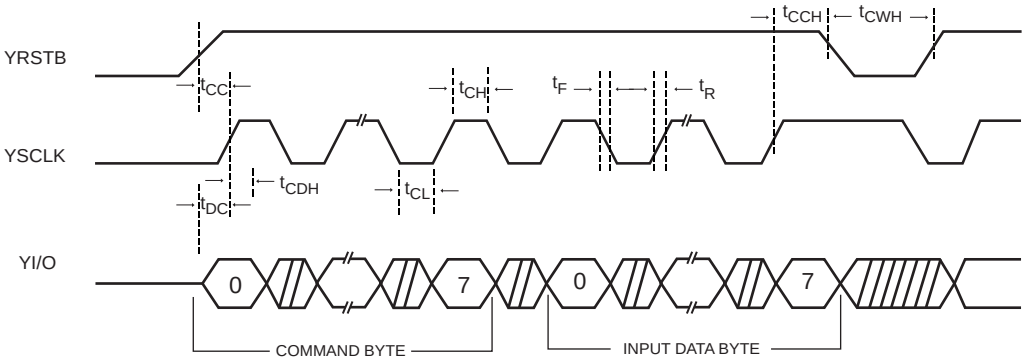
* For reading data byte from SHT1302 register, the first data bit to be transmitted at the first falling edge after the last bit of the command byte is written.

Timing Diagram

READ DATA TRANSFER



WRITE DATA TRANSFER



Application Diagram