HT6220A/HT6221A/HT6222A
Multi-Purpose Encoders

Features

- Operating voltage: 2.0V~3.6V
- DOUT with 38kHz carrier for IR medium
- Low standby current
- Minimum transmission word: one word
- Build-in RC (Internal RC) oscillator
- 16-bit address codes
- 8-bit data codes
- PPM code method
- Three double-active keys

- Maximum active keys
  - HT6220A: 30 keys
  - HT6221A: 32 keys
  - HT6222A: 64 keys
- Low power and high noise immunity CMOS technology
- HT6220A: 16-pin NSOP package
  HT6221A: 20-pin SOP package
  HT6222A: 24-pin SOP package

Applications

- Television , setup box and DVD player controllers
- Burglar alarm systems
- Smoke and fire alarm systems
- Garage door controllers

- Car door controllers
- Car alarm systems
- Security systems
- Other remote control systems

General Description

The devices are CMOS LSI encoders designed for use in remote control systems. They are capable of encoding 16-bit address codes and 8-bit data codes. Each address/data input can be set to one of the two logic states, 0 and 1.

The HT6220A/HT6221A/HT6222A contain 30keys (K1~K16, K17~K20, K33~K34, K37~K38, K41~K42, K45~K46, K49~K50), 32 keys (K1~K32) and 64 keys (K1~K64), respectively. When one of the keys is triggered, the programmed address/data is transmitted together with the header bits via an IR (38kHz carrier) transmission medium.

Block Diagram

Pin Assignment

HT6220A
16 NSOP-A

HT6221A
20 SOP-A
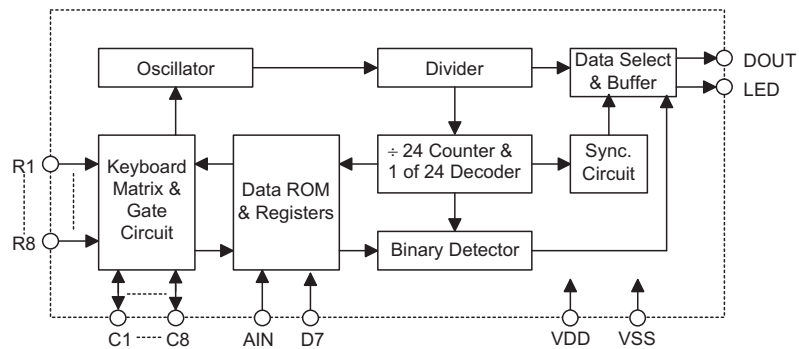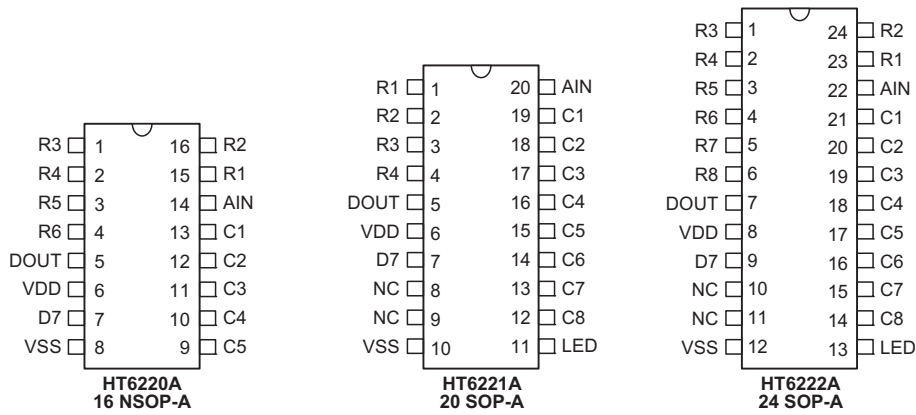
HT6222A
24 SOP-A

Pin Description

HT6222A

Pin No.	Pin Name	I/O	Internal Connection	Description
1~6	R3~R8	I	CMOS IN, Pull-low	Row control for keyboard matrix, active high
7	DOUT	O	NMOS OUT	Serial data output pin, with a 38kHz carrier
8	VDD	—	—	Positive power supply, 2.0V~3.6V for normal operation
9	D7	I	CMOS IN	Most significant data bit (D7) code setting
10, 11	NC	—	—	No connection
12	VSS	—	—	Negative power supply, ground
13	LED	O	CMOS OUT	Transmission enable indicator output
14~21	C8~C1	I/O	CMOS IN/OUT, Pull-low	Column control for keyboard matrix
22	AIN	I	CMOS IN, Pull-high Pull-low	Low byte address codes (8 bits) scan input
23~24	R1~R2	I	CMOS IN, Pull-low	Row control for keyboard matrix, active high

Approximate Internal Connection Circuits
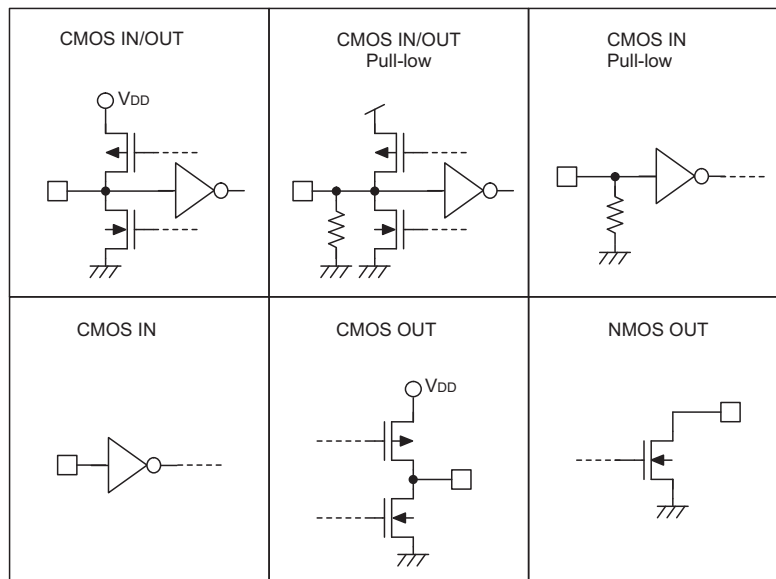
Absolute Maximum Ratings

Supply Voltage ....V_{SS}–0.3V to V_{SS}+6V

Input Voltage..............................V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature ....–50°C to 125°C

Operating Temperature............................–20°C to 75°C

Note: These are stress ratings only. Stresses exceeding the range specified under ″Absolute Maximum Ratings″ may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristic

Ta=25°C

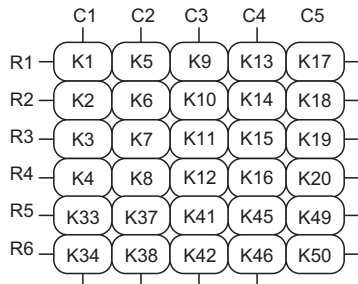| Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.0	3.0	3.6	V
I_{STB}	Standby Current	3V	Oscillator stops	—	0.1	1.0	μA
I_{DD}	Operating Current	3V	f_{OSC}=455kHz, no load	—	600	900	μA
I_{OL1}	Output Sink Current for DOUT	3V	V_O=0.6V	300	350	—	mA
I_{OH2}	Output Source Current for LED	3V	V_O=2.7V	−10	−60	—	μA
I_{OL2}	Output Sink Current for LED	3V	V_O=0.3V	1	2	—	mA
I_{OH3}	Output Source Current for C1~C8	3V	V_O=2.7V	−0.6	−2.0	—	mA
I_{OL3}	Output Sink Current for C1~C8	3V	V_O=0.3V	10	30	—	μA
V_{IH1}	Input High Voltage for R1~R8	3V	—	1.9	—	3.0	V
V_{IL1}	Input Low Voltage for R1~R8	3V	—	0	—	0.8	V
V_{IH2}	Input High Voltage for C1~C8	3V	—	1.6	—	3.0	V
V_{IL2}	Input Low Voltage for C1~C8	3V	—	0	—	0.6	V
V_{IH3}	Input High Voltage for AIN	3V	—	1.5	—	3.0	V
V_{IL3}	Input Low Voltage for AIN	3V	—	0	—	0.6	V
R_{PH1}	Input Pull-high Resistance for AIN	3V	V_{IN}=0V	100	200	400	kΩ
R_{PL1}	Input Pull-low Resistance for AIN	3V	V_{IN}=3V	70	150	250	kΩ
R_{PL2}	Input Pull-low Resistance for R1~R8	3V	V_{IN}=3V	120	200	320	kΩ
R_{PL3}	Input Pull-low Resistance for C1~C8	3V	V_{IN}=3V	300	500	1500	kΩ
f_{OSC}	System Frequency	3V	Ta=25°C	450.45	455	459.55	kHz
		2.0V~3.6V	0°C < Ta < 70°C	445.90	455	464.10	kHz

Note: f_{OSC} specification is guaranteed by design under 0°C < Ta < 70°C and not subject to production testing.
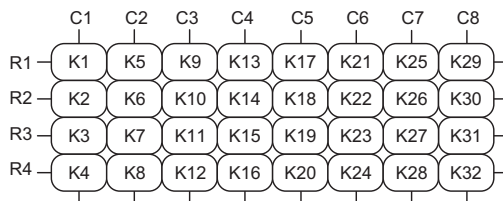
Functional Description

Keyboard Scan

The devices remain in the halt mode during the standby state (at this time, the oscillator stops, and the standby current<1μA). The HT6220A consists of 30 active keys, HT6221A has 32 active keys, and the HT6222A has 64 active keys. The keyboard forms of the devices are shown below.
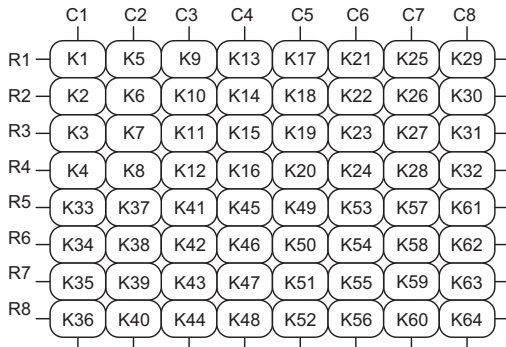
• The HT6220A keyboard form

	C1	C2	C3	C4	C5
R1	K1	K5	K9	K13	K17
R2	K2	K6	K10	K14	K18
R3	K3	K7	K11	K15	K19
R4	K4	K8	K12	K16	K20
R5	K33	K37	K41	K45	K49
R6	K34	K38	K42	K46	K50

• The HT6221A keyboard form

	C1	C2	C3	C4	C5	C6	C7	C8
R1	K1	K5	K9	K13	K17	K21	K25	K29
R2	K2	K6	K10	K14	K18	K22	K26	K30
R3	K3	K7	K11	K15	K19	K23	K27	K31
R4	K4	K8	K12	K16	K20	K24	K28	K32

• The HT6222A keyboard form

|	C1	C2	C3	C4	C5	C6	C7	C8
R1	K1	K5	K9	K13	K17	K21	K25	K29
R2	K2	K6	K10	K14	K18	K22	K26	K30
R3	K3	K7	K11	K15	K19	K23	K27	K31
R4	K4	K8	K12	K16	K20	K24	K28	K32
R5	K33	K37	K41	K45	K49	K53	K57	K61
R6	K34	K38	K42	K46	K50	K54	K58	K62
R7	K35	K39	K43	K47	K51	K55	K59	K63
R8	K36	K40	K44	K48	K52	K56	K60	K64

When one of the keys (30, 32 or 64 keys) is triggered for over 36ms, the oscillator is enabled and the chip is activated. If the key is pressed and held for 108ms or less, the 108ms transmission codes are enabled and comprised of a header code (9ms), an off code (4.5ms), low byte address codes (9ms~18ms), high byte address codes (9ms~18ms), 8-bit data codes (9ms~18ms), and the inverse codes of the 8-bit data codes (18ms~9ms). After the pressed key is held for 108ms, if the key is still held down, the transmission codes turn out to be a composition of header (9ms) and off codes (2.24ms) only.

To avoid mistakes made by keyboard scanning or simultaneous two-key inputs (except for the three double-key active functions (K21+K22, K21+K23, and K21+K24), the devices are facilitated with 36ms starting time.

The HT6221A/HT6222A also provide three double-key active functions (K21+K22, K21+K23, and K21+K24) for tape deck recording operations. The double-key operation rules are shown in timing 4 and timing 6.
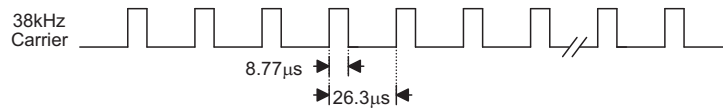
Transmission Codes

The transmission codes of the devices consist of a 9ms header code, a 4.5ms off code, 16-bit address codes (18ms~36ms), 9ms~18ms 8-bit data codes, and the inverse code of the 8-bit data codes. The following is an illustration of the transmission codes.
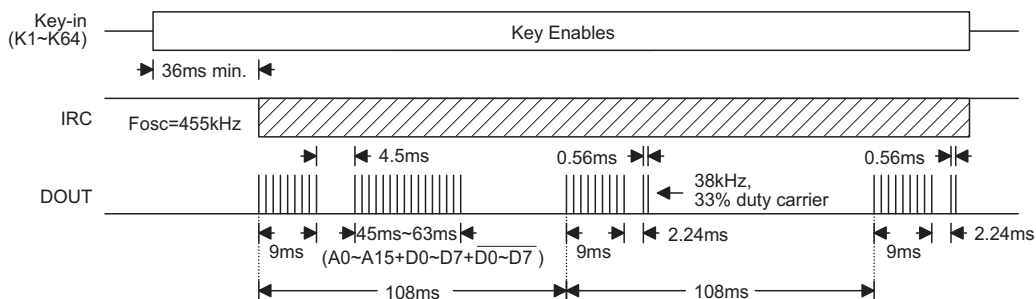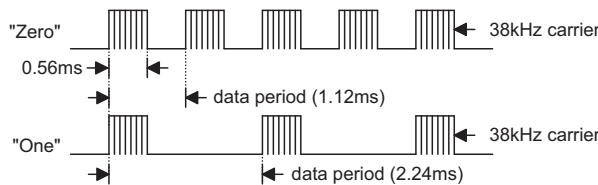

Timing 1. Output Format for the DOUT

The output code carrier of the DOUT pin is shown in Timing 2.

Timing 2. 38kHz Carrier

The transmission codes employ the PPM (Pulse Position Modulation) method to represent their two logic states by ″0″ (1.12ms) and ″1″ (2.24ms) as shown in Timing 3.
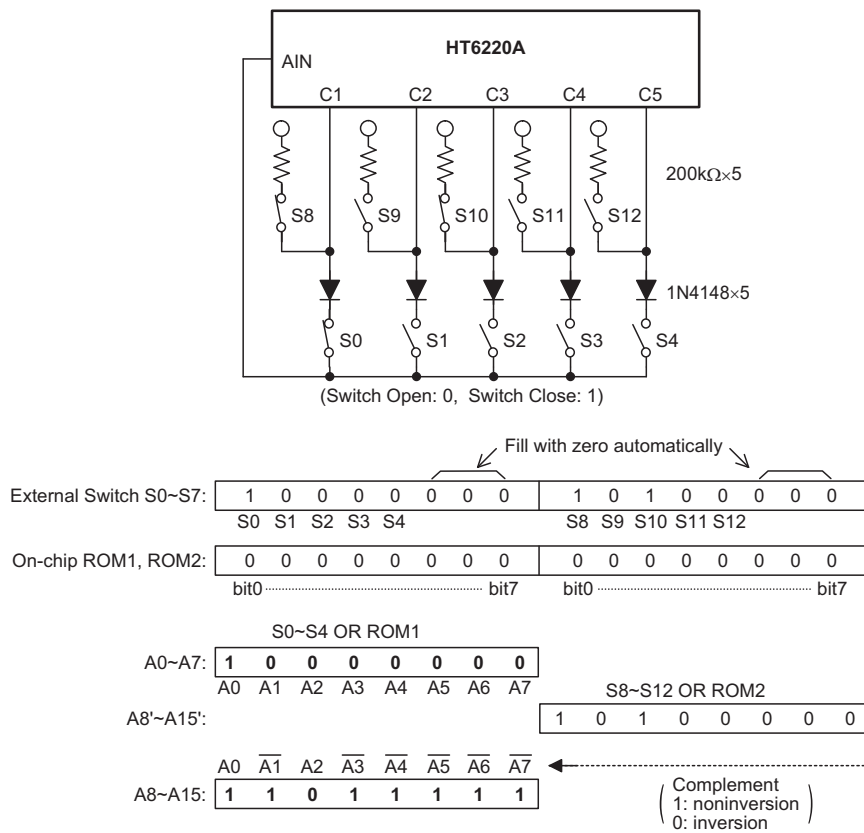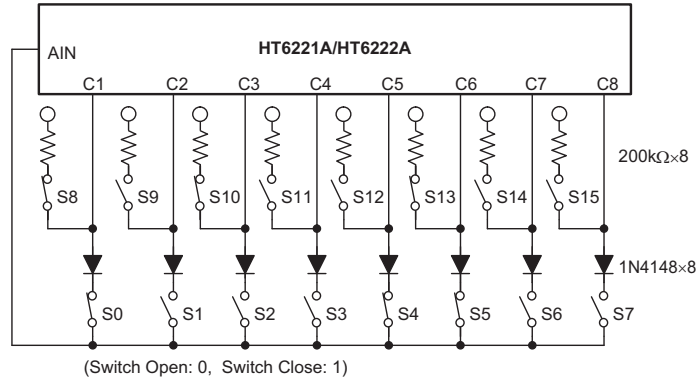

Timing 3. Logic States

• Setting the address codes (A0~A15)

The algorithm rule of the address codes (A0~A15) can be selected by mask option.

In this case, the 16-bit on-chip MASK ROM (ROM1 and ROM2) are available, and the value of ROM1 (8 bits) and ROM2 (8 bits) are decided by one MASK LAYER. The current value of ROM1 and ROM2 are both ″00H″. The A0~A7 are set by logical OR between the external switch S0~S7 and the ROM1. The A8~A15 equal some bits inverted to A0~A7, the inversion are decided by Logical OR between the external switch S8~S15 and the ROM2.

For example:
The following is an illustration of these rules in selecting the address codes (A0~A15).

(Switch Open: 0, Switch Close: 1)

HT6221A/HT6222A

AIN

C1 C2 C3 C4 C5 C6 C7 C8

S8 S9 S10 S11 S12 S13 S14 S15

200kΩ×8

1N4148×8

S0 S1 S2 S3 S4 S5 S6 S7

(Switch Open: 0, Switch Close: 1)

External Switch S0~S15:	1	0	0	0	1	1	0	0		1	0	1	0	0	1	0	0
	S0	S1	S2	S3	S4	S5	S6	S7		S8	S9	S10	S11	S12	S13	S14	S15

On-chip ROM1, ROM2:	0	0	0	0	0	0	0	0		0	0	0	0	0	0	0	0
	bit0							bit7		bit0							bit7

S0~S7 OR ROM1

A0~A7:	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**0**
	A0	A1	A2	A3	A4	A5	A6	A7

S8~S15 OR ROM2

A8'~A15':	1	0	1	0	0	1	0	0

	A0	$\overline{A1}$	A2	$\overline{A3}$	$\overline{A4}$	A5	$\overline{A6}$	$\overline{A7}$
A8~A15:	**1**	**1**	**0**	**1**	**0**	**1**	**1**	**1**

Complement
1: noninversion
0: inversion

- Values of the data codes (D0~D7)

  The HT6220A/HT6221A/HT6222A contain 30, 32 and 64 active keys, respectively. Each key corresponds to a data code. For tape deck recording, the HT6221A/HT6222A provide three double-key functions. The double-key, single-key, and double-key operation rules are shown in Table 3, Table 4, Timing 4, Timing 5 and Timing 6.

Table 3: Double-key data code table

KEY	Data Codes D0~D6	Data Code D7
K21 + K22	1010110	0/1
K21 + K23	0110110	0/1
K21 + K24	1110110	0/1

Note: D7 is defined by an external switch

Table 4: K1~K64 single-key data code table

KEY	Data Codes D0~D6	Data Code D7	KEY	Data Codes D0~D6	Data Code D7
K1	0000 000	0/1	K33	0000 001	0/1
K2	1000 000	0/1	K34	1000 001	0/1
K3	0100 000	0/1	K35	0100 001	0/1
K4	1100 000	0/1	K36	1100 001	0/1
K5	0010 000	0/1	K37	0010 001	0/1
K6	1010 000	0/1	K38	1010 001	0/1
K7	0110 000	0/1	K39	0110 001	0/1
K8	1110 000	0/1	K40	1110 001	0/1
K9	0001 000	0/1	K41	0001 001	0/1
K10	1001 000	0/1	K42	1001 001	0/1
K11	0101 000	0/1	K43	0101 001	0/1
K12	1101 000	0/1	K44	1101 001	0/1
K13	0011 000	0/1	K45	0011 001	0/1
K14	1011 000	0/1	K46	1011 001	0/1
K15	0111 000	0/1	K47	0111 001	0/1
K16	1111 000	0/1	K48	1111 001	0/1
K17	0000 100	0/1	K49	0000 101	0/1
K18	1000 100	0/1	K50	1000 101	0/1
K19	0100 100	0/1	K51	0100 101	0/1
K20	1100 100	0/1	K52	1100 101	0/1
K21	0010 100	0/1	K53	0010 101	0/1
K22	1010 100	0/1	K54	1010 101	0/1
K23	0110 100	0/1	K55	0110 101	0/1
K24	1110 100	0/1	K56	1110 101	0/1
K25	0001 100	0/1	K57	0001 101	0/1
K26	1001 100	0/1	K58	1001 101	0/1
K27	0101 100	0/1	K59	0101 101	0/1
K28	1101 100	0/1	K60	1101 101	0/1
K29	0011 100	0/1	K61	0011 101	0/1
K30	1011 100	0/1	K62	1011 101	0/1
K31	0111 100	0/1	K63	0111 101	0/1
K32	1111 100	0/1	K64	1111 101	0/1

Note: D7 is defined by an external switch
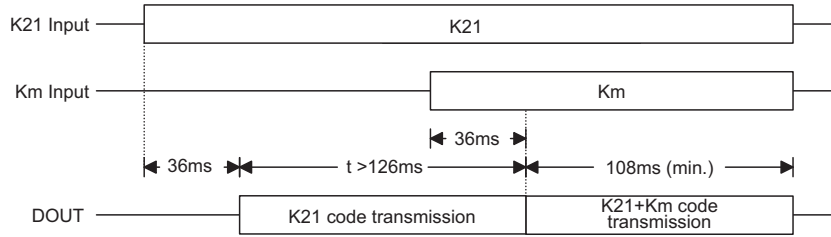
    D7=0 : connect to VDD

    D7=1 : connect to VSS

K21 Input ──── | K21 |

Km Input ──── | Km |

36ms< t <126ms ──── 36ms

36ms ──── 108ms (min.)

DOUT ──── | K21 code transmission |

(a)

K21 Input ──── | K21 |

Km Input ──── | Km |

0< t <36ms

DOUT ──── No transmission

(b)

K21 Input ──── | K21 |

0< t <36ms

Km Input ──── | Km |

DOUT ──── No transmission

(c)

K21 Input ──── | K21 |

Km Input ──── | Km |

36ms< t <126ms ──── 36ms

36ms ──── 108ms (min.)

DOUT ──── | Km code transmission |

(d)
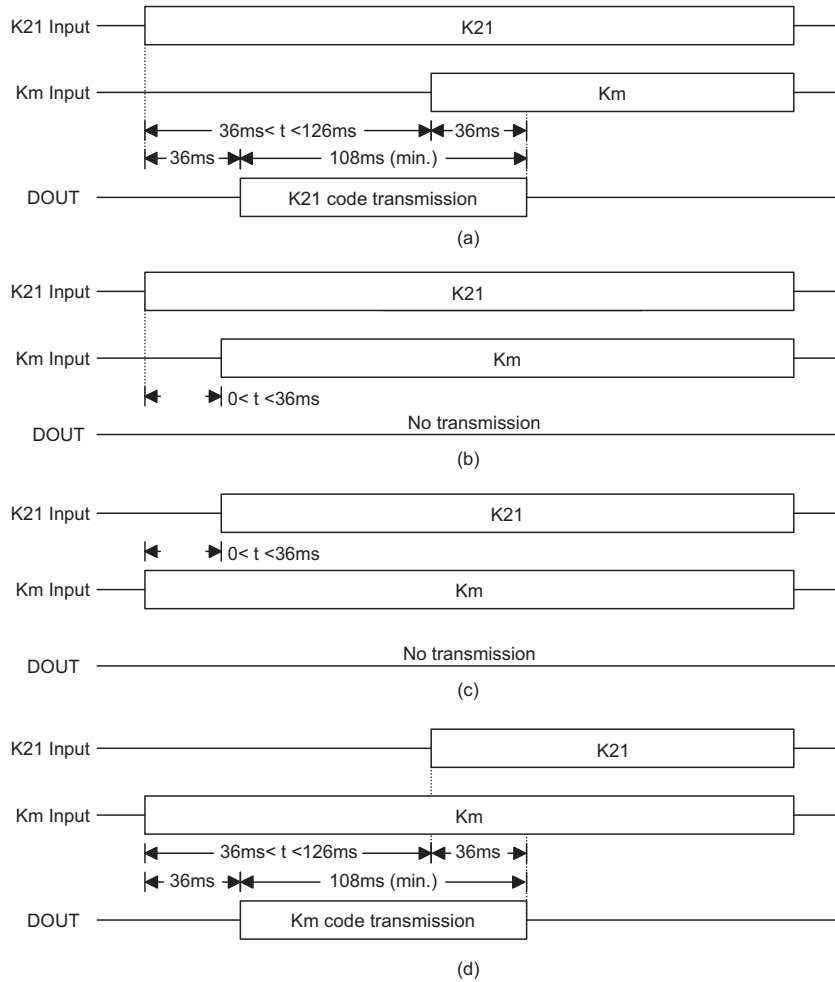
Timing 4. Invalid Double-Key Input

Kn Input ──── | Kn |

36ms ──── t >108ms

DOUT ──── | Kn code transmission |

(a)

Kn Input ──── | Kn |

t <108ms

36ms ──── 108ms

DOUT ──── | Kn code transmission |

(b)
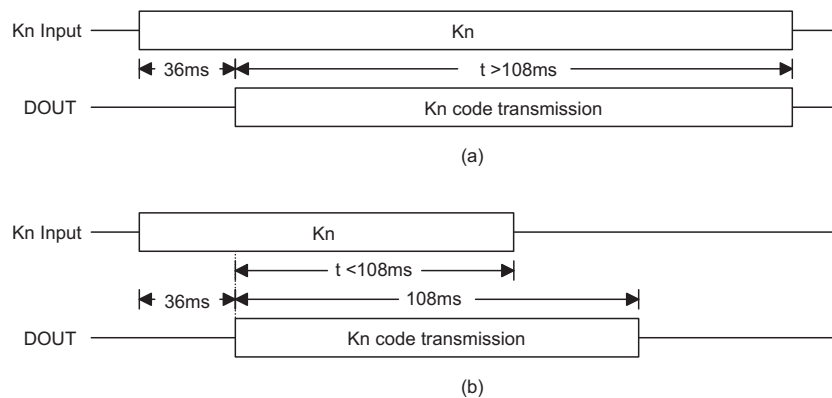
Note: Kn can be one of K1~K64

Timing 5. Valid Single-Key Input

Note: Km can be one of K22~K24

Timing 6. Valid Double-Key Input

DOUT and IR LED

After the transmission codes are sent, the DOUT pin generates transmission codes with a carrier, and the IR-LED goes low to drive a transmission indicator. The DOUT pin abbreviate exterior transistor, to provide large current driving ability.

IRC

The frequency of the internal RC(IRC) oscillator is depending on the temperature and operating voltage.

At Ta=25°C at 3.0V, the IRC has an accuracy of ±1 per cent. In the range of 0°C to 70°C at 2.0V~3.6V, the accuracy value of the RC frequency increases to the maximum value of ±2 per cent.

Application Circuits

HT6220A Application Circuit
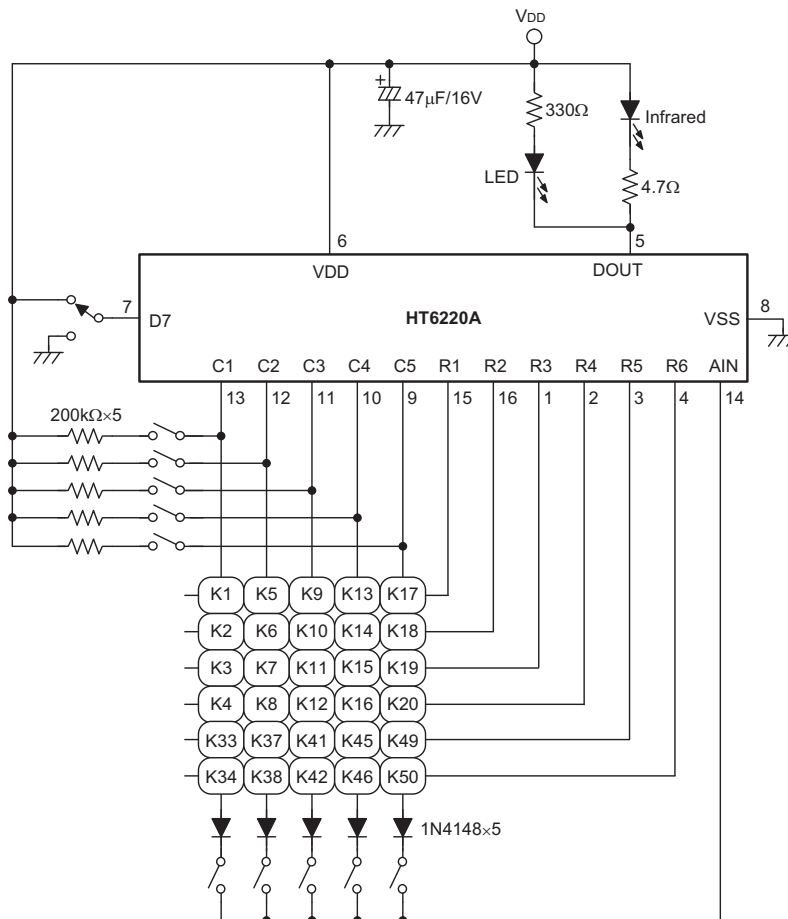
Note: Typical infrared diode: EL-1L2 (KODENSHI CORP.)

HT6221A Application Circuit
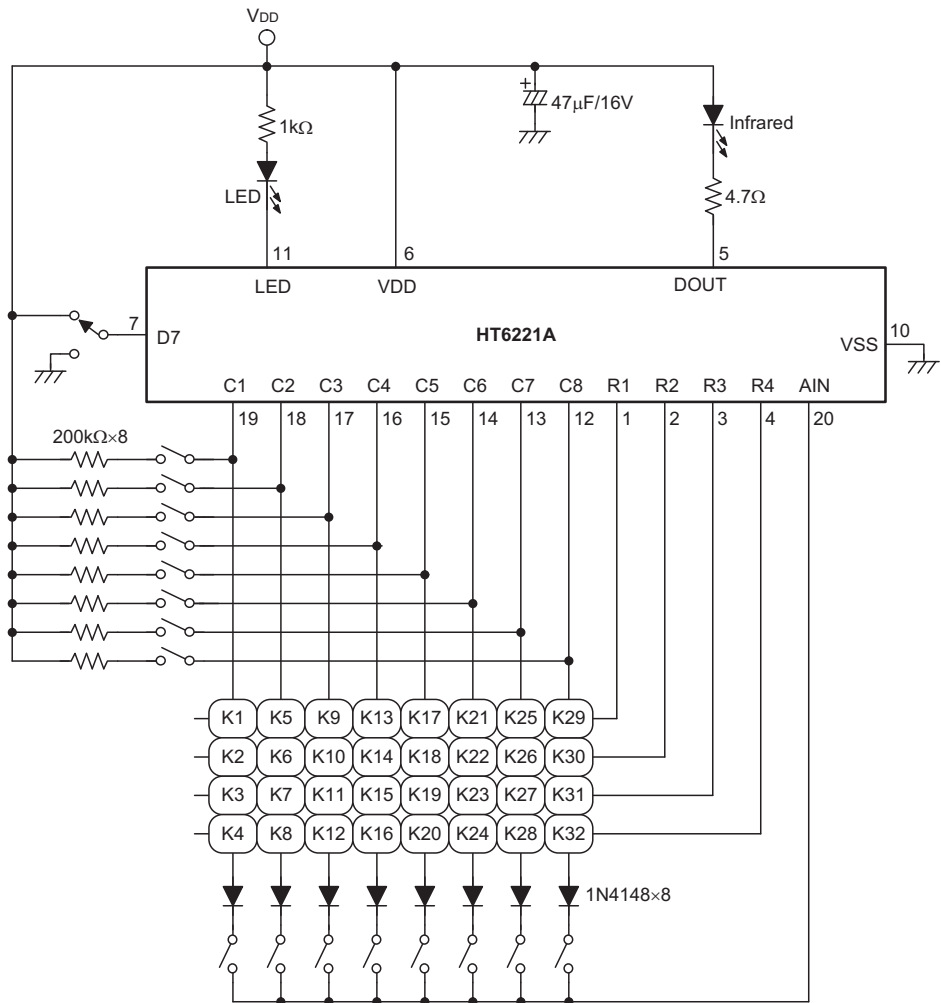
Note: Typical infrared diode: EL-1L2 (KODENSHI CORP.)

HT6222A Application Circuit
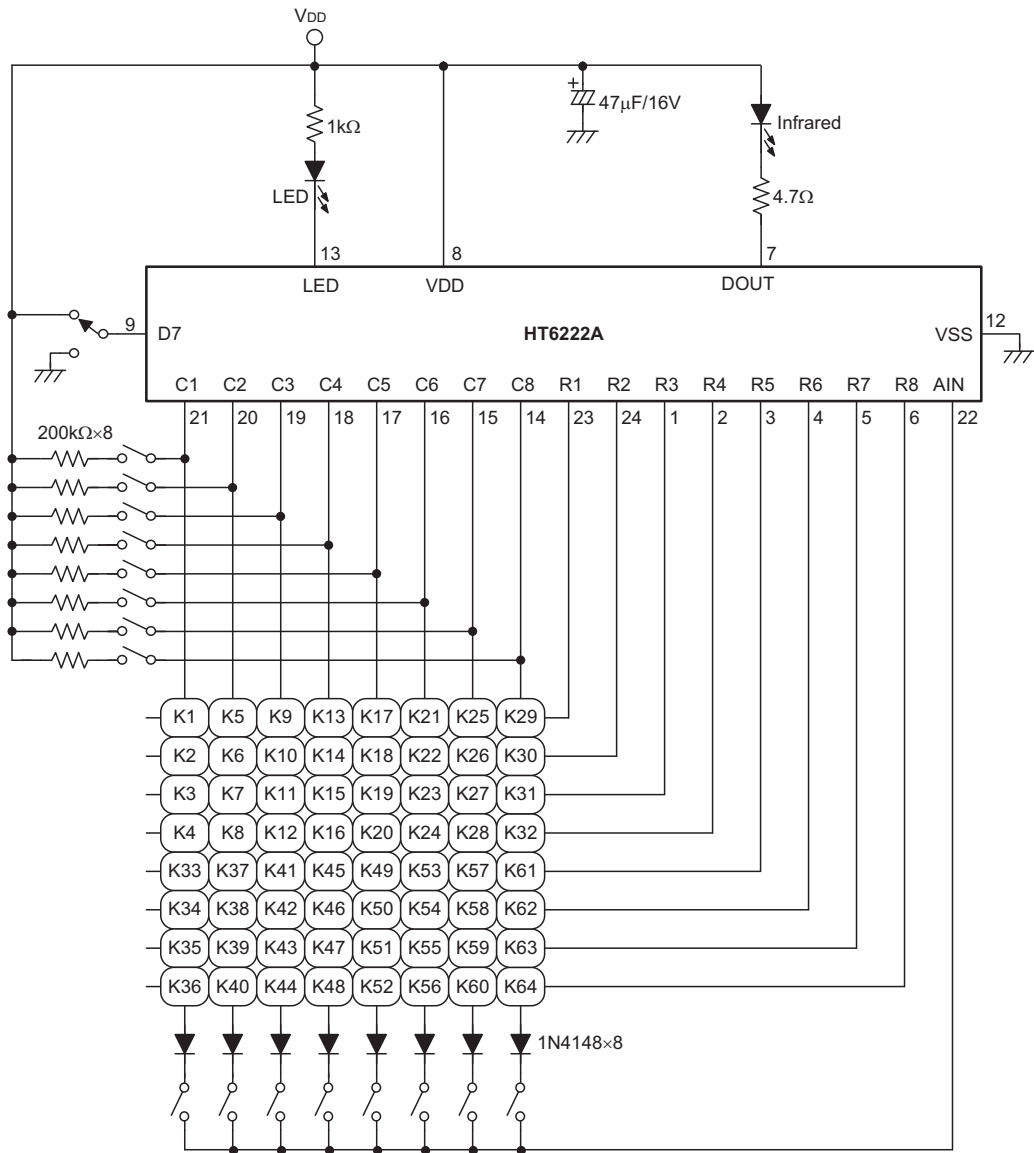
Note: Typical infrared diode: EL-1L2 (KODENSHI CORP.)

Package Information

16-pin NSOP (150mil) Outline Dimensions
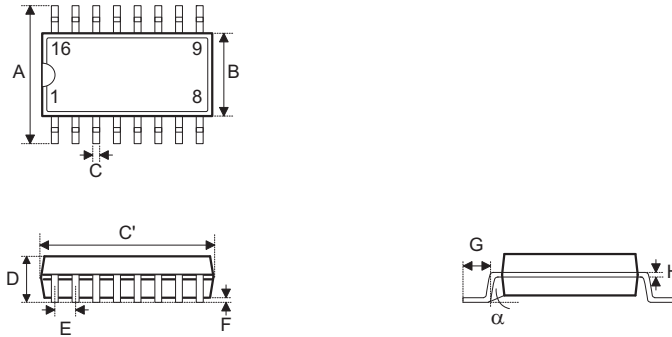
• MS-012

Symbol	Dimensions in mil		
	Min.	**Nom.**	**Max.**
A	228	—	244
B	150	—	157
C	12	—	20
C′	386	—	394
D	—	—	69
E	—	50	—
F	4	—	10
G	16	—	50
H	7	—	10
α	0°	—	8°

20-pin SOP (300mil) Outline Dimensions
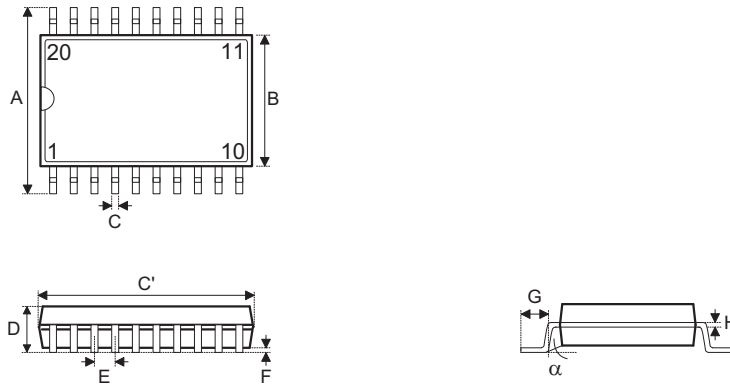
- MS-013

Symbol	Dimensions in mil		
	Min.	**Nom.**	**Max.**
A	393	—	419
B	256	—	300
C	12	—	20
C′	496	—	512
D	—	—	104
E	—	50	—
F	4	—	12
G	16	—	50
H	8	—	13
α	0°	—	8°

24-pin SOP (300mil) Outline Dimensions
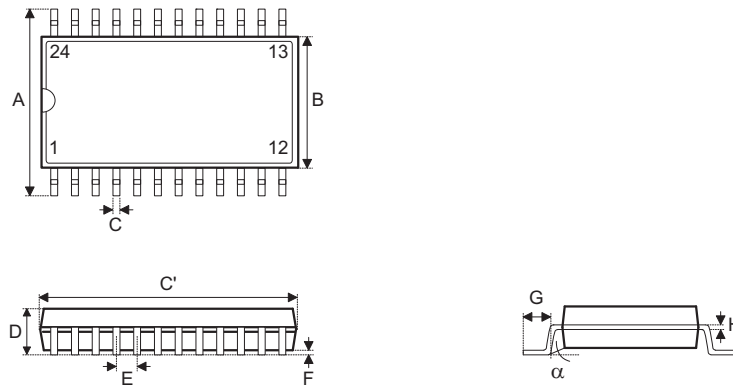
• MS-013

Symbol	Dimensions in mil		
	Min.	**Nom.**	**Max.**
A	393	—	419
B	256	—	300
C	12	—	20
C′	598	—	613
D	—	—	104
E	—	50	—
F	4	—	12
G	16	—	50
H	8	—	13
α	0°	—	8°

Product Tape and Reel Specifications

Reel Dimensions
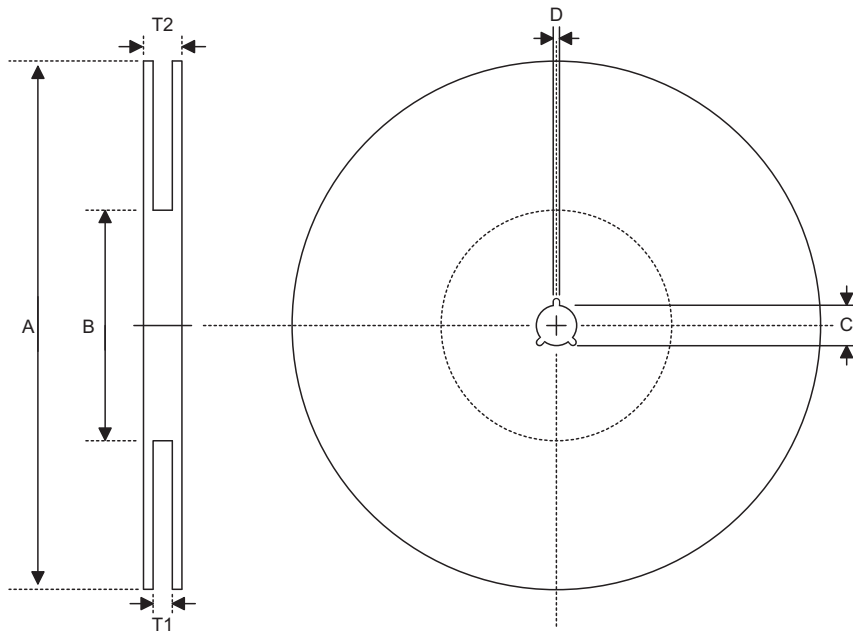
SOP 16N (150mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	16.8 $^{+0.3/-0.2}$
T2	Reel Thickness	22.2±0.2

SOP 20W, SOP 24W

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	24.8 $^{+0.3/-0.2}$
T2	Reel Thickness	30.2±0.2

Carrier Tape Dimensions
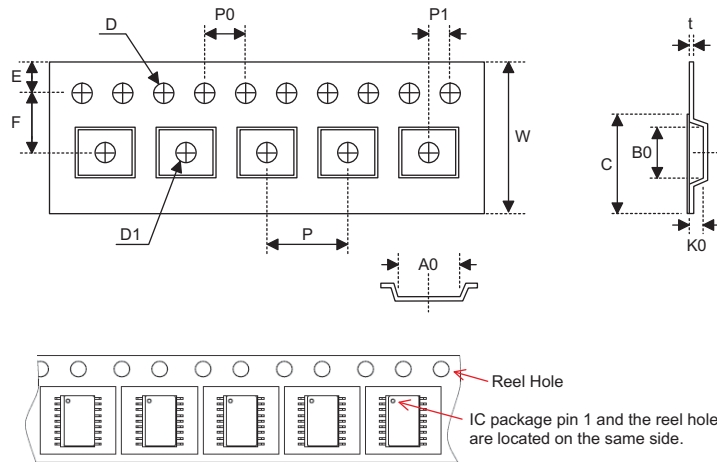
SOP 16N (150mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0±0.3
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	1.55 +0.10/-0.00
D1	Cavity Hole Diameter	1.50 +0.25/-0.00
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.5±0.1
B0	Cavity Width	10.3±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	13.3±0.1

SOP 20W

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0 +0.3/-0.1
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.5 +0.1/-0.0
D1	Cavity Hole Diameter	1.50 +0.25/-0.00
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.8±0.1
B0	Cavity Width	13.3±0.1
K0	Cavity Depth	3.2±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	21.3±0.1

SOP 24W

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.55 $^{+0.10/-0.00}$
D1	Cavity Hole Diameter	1.50 $^{+0.25/-0.00}$
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.9±0.1
B0	Cavity Width	15.9±0.1
K0	Cavity Depth	3.1±0.1
t	Carrier Tape Thickness	0.35±0.05
C	Cover Tape Width	21.3±0.1