PNI 11096

3-Axis Magneto-Inductive Sensor Driver and Controller with SPI Serial Interface

General Description

The PNI 11096 is a low cost magnetic Measurement Application Specific Integrated Circuit (ASIC) designed for use with PNI Corporation's magneto-inductive sensors. The PNI 11096 can control and measure three independent magneto-inductive sensors. Each sensor is individually selectable for measurement, and can also be individually configured for measurement resolution. The PNI 11096 has diagnostic modes and outputs to test the oscillator and counter circuits.

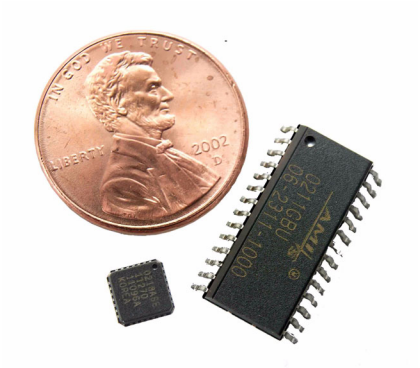
The PNI 11096 contains the entire measurement circuit, both analog and digital sections. Each sensor changes its inductance with an applied change in magnetic field parallel to the sensor. In order to make a measurement, the sensor is switched into an LR oscillator circuit. The bipolar differential measurement scheme used by the PNI 11096 makes the magnetic measurement inherently temperature independent. It also has the benefit of transforming the measurement range into a zero centered, positive/negative value.

Features

- Low supply current:
  <500 µA at 3 VDC
  <1 µA, idle mode
- Complete 3-axis magnetic sensor driver
- Ultra-low magnetic signature in Die form
- Flexible supply voltage: 2.2 to 5.0 V
- Fast sample rate: up to 2000 samples/second
- Wide dynamic range: 96 dB (16 bits) in hardware with 18 dB (3 bits) additional gain scaling available
- Fully digital interface: SPI protocol

Applications

- Compassing
- Magnetometer instruments
- Magnetic object sensing
- Magnetic ink sensing



Ordering Information

Name	Part Number	Package
26 pad Die	10174	each
28 pin SOIC	10175	each
28 pin MLF	11182	each

Specifications

CAUTION

Stresses beyond those listed under Table 1 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum
V_{DD}	DC supply voltage	–0.3 VDC	5.25 VDC
V_{IN}	Input pin voltage	V_{DD} – 0.3 VDC	V_{DD} + 0.3 VDC
I_{IN}	Input pin current	–10 mA at 25 °C	10 mA at 25 °C
T_{STRG}	Storage temperature	–40 °C	125 °C

Table 2. Supply Operating Conditions

Symbol	Parameter	Minimum	Maximum
V_{DD}	Digital DC Supply	2.2 VDC	5.0 VDC
I_{DD} (nominal)	Idle (V_{DD} = 3 VDC)		0.1 mA
I_{DD} (maximum)	Operating (V_{DD} = 3 V, SEN-S65)		0.5 mA
ILKSTBY[a]	I_{DD} @ VSTBY pin		100 nA
V_{SS}	Digital Ground	0 V	0 V
TA	Ambient Temperature	–20 °C	70 °C

a. VSTBY = 5.5V, $AV_{DD} = DV_{DD} = AV_{SS} = DV_{SS}$ = 0 V, Temperature 27 °C

Electrical Specifications

Parameter voltage and current levels

Testing for the currents listed in Table 3 assume a static test setup with measurements performed while static data is applied to the device. Test type parameters apply as listed in theTable 7 on page 7.

Table 3. Inputs

Test Type	Vil[a]	Vih[a]	Iil[b]	Iih[b]
AIB (analog input)	0.2 V	2.0 V	0.0 to –1.0 µA	0.0 to 1.0 µA
IBA (CMOS)	0.25 V	0.8 V	0.0 to –1.0 µA	0.0 to 1.0 µA
IBT (CMOS, SC Hsy = 1.0)[c]	0.2 V	0.8 V	0.0 to –1.0 µA	0.0 to 1.0 µA

a. CMOS values are V_{IN} x V_{DD}.
b. Iil and Iih are tested at V_{DD} = 3.6 V. Not tested at less than room temperature.
c. SC = Schmitt

Table 4. Outputs

Test Type	Vol	Voh	Iol[a]	Ioh[a]
OB1[b]	<0.4 V	>2.4 V	1.0 mA minimum	–1.0 mA minimum
OB2[b]	<0.4 V	> 2.4 V	1.0 mA minimum	–1.0 mA minimum
OB3[c]	0.267 V	1.936 V	10 mA minimum	–10 mA minimum

a. Polarity on currents indicate direction of current (+) for sinking (–) for sourcing.
b. V_{DD} = 4.5 to 5.0 V.
c. V_{DD} = 2.2 V

Table 5. I/0 Pins

Test Type	Vil[a]	Vih[a]	Vol[b]	Voh[b]	Iol[b]	Ioh[b]	Ioz[c]	Ioz[c]
IO1A CMOS	0.30 V	0.70 V	0.40 V	4.1 V	–0.64 mA	0.15 µA	39 µA minimum	217 µA maximum

a. CMOS values are V_{IN} x V_{DD}.
b. Tested at V_{DD} = 4.8 V.
c. Tested with V_{DD} = 5.2 V. Leakage on I/0 pins is typically checked for ±2 µA with the output device turned off and no PU or PD.

Theory of Operation

The PNI 11096 contains the entire measurement circuitry necessary to use PNI Corporation's magneto-inductive sensors. Each sensor changes its inductance with a change in magnetic field parallel to the sensor. To make a measurement, the sensor is switched into an LR oscillator circuit. One side of the sensor is grounded; the other side is alternately driven with positive and negative current through the oscillator circuit (that is, forward bias). The PNI 11096 will then switch the bias connections to the sensor and make another measurement. The side that was previously grounded is now charged and discharged; the other side is now ground (that is, reverse bias).

Figure 1 illustrates the change between these two measurements. The actual magnetic measurement is the difference between these two measurements. This measurement scheme is used to make the magnetic measurement temperature independent. It also has the benefit of transforming the measurement range into a zero centered, positive/negative value.

The PNI 11096 returns the data to the host microprocessor over the SPI interface. The microprocessor simply asks the PNI 11096 for data from a specific axis, and the PNI 11096 returns the data in a 16-bit 2's compliment format.

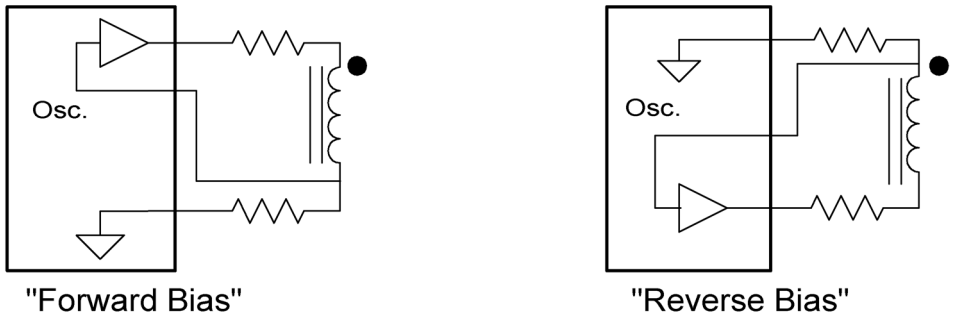


Figure 1. Forward Bias versus Reverse Bias

Connections

A typical connection configuration is shown in Figure 2 with the analog and digital sections of the PNI 11096 tied together. This configuration is adequate for compassing applications. For higher performance applications where less noise is desirable, separating the sections is recommended. The PNI 11096 can control up to three sensors; if less are needed, the unneeded pins should be left to float.

The VSTBY pin must always be equal to or higher than any voltage present on any other 11096 pin. VSTBY is connected to the cathode end of a diode in the array. The anode end of each diode in the array is connected to each of the digital interface signal pins. Leaving VSTBY floating or connected to ground when other pins are potentially active, as in multiplexed SPI networks, will cause excessive current drain.

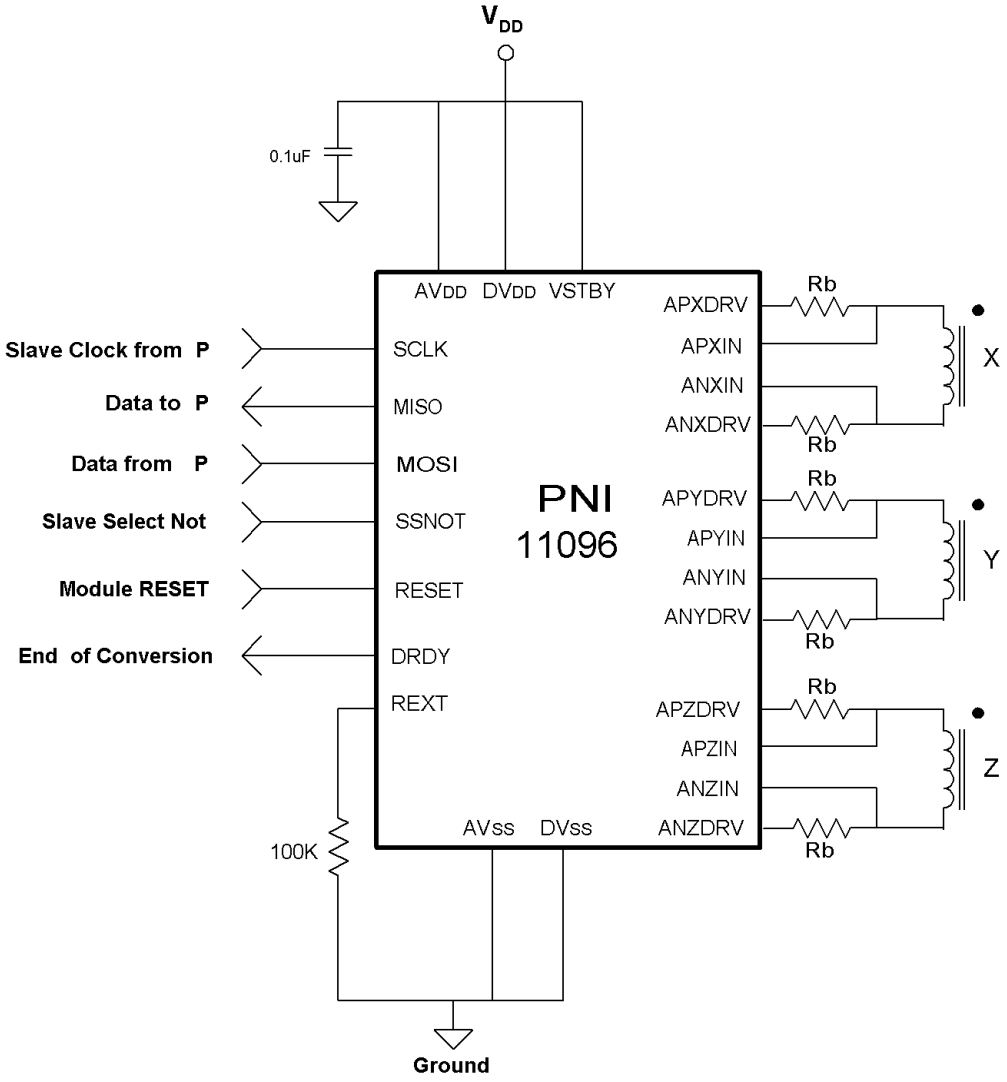


Figure 2. Typical Connection

Table 6. Rb Value Sufficient for Evaluation

	SEN-L	SEN-S
5 VDC	150 Ohm	75 Ohm
3 VDC	100 Ohm	43 Ohm

Host Processor Interface

All accesses to and from the PNI 11096 are through a hardware handshaking, synchronous serial interface that adheres to the Motorola SPI protocol. The interface consists of six signals; SCLK, MOSI, MISO, SSNOT, RESET and DRDY.

Table 7. Pin Definition

28 SOIC (pin number)	26 DIE (pin number)	28 MLF (pin number)	Pin Name	I/O Type[a]	Test Type Parameters	Description
1	1	26	VSTBY	DP	V_{DD}	Input protection clamp diode. Connect to V_{DD}
2	2	27	SCLK	DI	IBT	Serial clock input for SPI port. 1 MHz maximum (Rext = 100 kHz).
3	3	28	MISO	DO	OB2	Serial data output (Master In Slave Out)
4	4	1	MOSI	DI	IBA	Serial data output (Master Out Slave In)
5	5	3	SSNOT	DI	IBA	Active low chip select for SPI port
6	----	2				Not connected
7	6	4	AV_{DD}	AP	V_{DD}	Supply voltage for analog section
8	7	5	AV_{SS}	AP	V_{SS}	Ground pin for analog section
9	8	6	+ZDRV	DO	OB3	Z sensor drive output
10	9	7	+ZIN	AI	AIB	Z sensor sense input
11	10	8	–ZIN	AI	AIB	Z sensor sense input
12	11	9	–ZDRV	DO	OB3	Z sensor drive output
13	12	10	+YDRV	DO	OB3	Y sensor drive output
14	13	11	+YIN	AI	AIB	Y sensor sense input
15	14	12	DV_{DD}	DP	V_{DD}	Supply voltage for digital section
16	15	13	–YIN	AI	AIB	Y sensor sense input
17	16	14	–YDRV	DO	OB3	Y sensor drive output
18	17	15	+XDRV	DO	OB3	X sensor drive output
19	18	16	+XIN	AI	AIB	X sensor sense input
20	19	17	–XIN	AI	AIB	X sensor sense input

Table 7. Pin Definition

28 SOIC (pin number)	26 DIE (pin number)	28 MLF (pin number)	Pin Name	I/O Type[a]	Test Type Parameters	Description
21	20	18	–XDRV	DO	OB3	X sensor drive output
22	21	19	DV_{ss}	DP	V_{SS}	Ground pin for digital section
23	----	20				Not connected
24	22	21	COMP	DO	OB1	Comparator output. Used for diagnostics.
25	23	22	RESET	DI	IBA	Reset input
26	24	23	DRDY	DO	OB1	Data ready
27	25	24	DHST	DIO	IO1A	High speed oscillator output. Output is 1/2 clock speed. Used for diagnostics.
28	26	25	REXT	AI	AIB	External timing resistor for high speed clock. 100 k ohm typical.

a. I/O types: D = digital, A = analog, I = input, O = output, IO = bidirectional, and P = power pad.

SPI Port Line Descriptions

MOSI
Master In Slave Out

The data sent to the PNI 11096. Data is transferred most significant bit first. The MOSI line will accept data once the SPI is enabled by taking SSNOT low. Valid data must be presented at least 100 nS before the rising edge of the clock, and remain valid for 100 nS after the edge. New data may be presented to the MOSI pin on the falling edge of SCLK.

SSNOT
Slave Select

Selects the PNI 11096 as the operating slave device. The SSNOT line must be low prior to data transfer and must stay low during the entire transfer. Once the command byte is received by the PNI 11096, and the PNI 11096 begins to execute the command, the SSNOT line can be deselected until the next SPI transfer.

SCLK
Serial Clock

Used to synchronize both the data in and out through the MISO and MOSI lines. SCLK is generated by a master device. SCLK should be 1 MHz or less. The PNI 11096 is configured to run as a slave device, making it an input. One byte of data is exchanged over eight clock cycles. Data is captured by the master device on the rising edge of SCLK. Data is shifted out and presented to the PNI 11096 on the MOSI pin on the falling edge of SCLK.

MISO
Master In Slave Out

The data sent from the PNI 11096 to the master. Data is transferred most significant bit first. The MISO line is placed in a high impedance state if the slave is not selected (SSNOT = 1).

Hardware Handshaking Line Descriptions

RESET

RESET is usually low. RESET must be toggled from low-high-low.

DRDY
Data Ready

DRDY is low after a RESET; after a command has been received and the data is ready, DRDY will be high. It is recommended that the DRDY line always be used to ensure that the data is clocked out of the PNI 11096 only when it is available. If it is determined that the DRDY line cannot be used due to lack of I/O lines to the host processor, then the times listed in Table 8 can be used to set open-loop wait times. The values listed are the maximum delays from the end of the SCLK command until the rise of the DRDY at each period select setting. The maximum delay occurs when the sensor being sampled is in a zero field.

Table 8. Maximum Delay for DRDY

Period Select	Maximum Delay	
	SEN-S65 (3 VDC)	**SEN-L (3 VDC)**
/32	500 µS	1.4 mS
/64	1.0 mS	2.5 mS
/128	2.0 mS	4.5 mS
/256	4.0 mS	8.0 mS
/512	7.5 mS	15.5 mS
/1024	15 mS	30.5 mS
/2048	35.5 mS	60.5 mS
/4096	60 mS	120.0 mS

Operation

Basic operation will follow these steps. Refer to Figure 3 and Figure 4.

1. SSNOT is brought low.
2. Pulse RESET high (return to low state). You must RESET the PNI 11096 before every measurement.
3. Data is clocked in on the MOSI line. Once eight bits are read in, the PNI 11096 will execute the command.
4. The PNI 11096 will make the measurement. A measurement consists of forward biasing the sensor and making a period count; then reverse biasing the sensor and counting again; and finally, taking the difference between the two bias directions.
5. At the end of the measurement, the DRDY line is set to high indicating that the data is ready. In response to the next 16 SCLK pulses, data is shifted out on the MISO line.

If you need to make another measurement, go to Step 2. You can send another command after the reset. In this case, keep SSNOT low. If you will not be using the PNI 11096, set SSNOT to high to disable the SPI port.

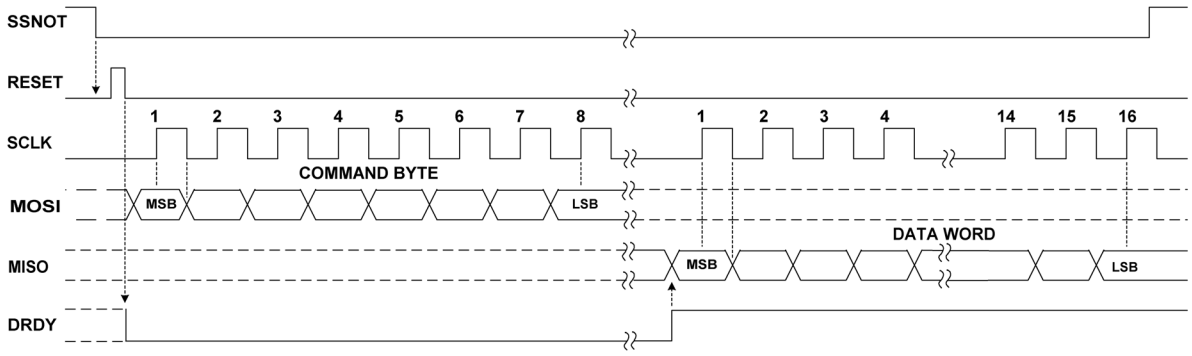


Figure 3. SPI Port Full Timing Sequence (cpol = 0)

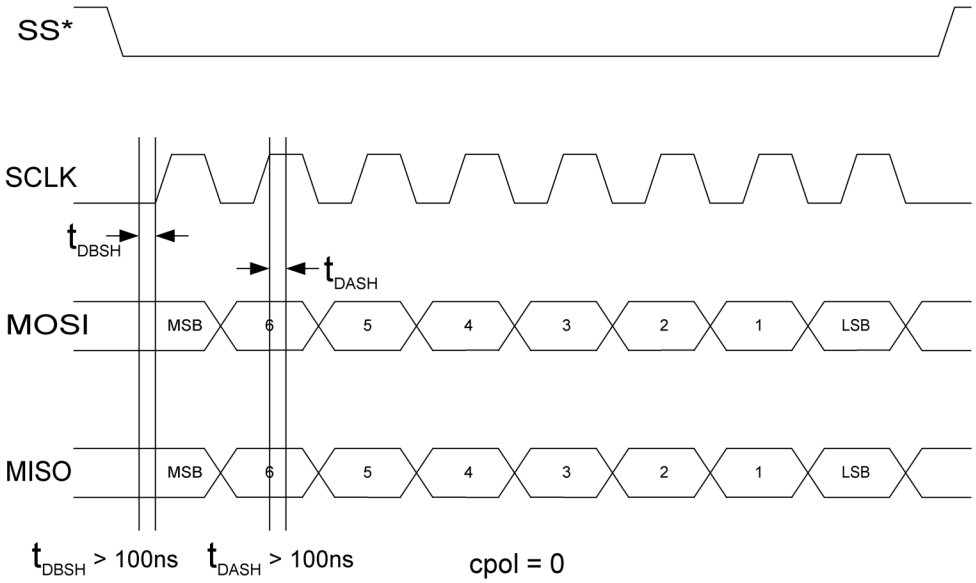


Figure 4. SPI Port Timing Parameters (cpol = 0)

SPI Port Usage Tips

A SPI port can be implemented using different clock polarity options. The clock polarity used with the PNI 11096 must be normally low, (***cpol = 0***). Figure 4 graphically shows the timing sequence (***cpol = 0***). Data is always considered valid while the SCLK is high (t_{DASH} = Time, Data After SCLK High). When SCLK is low, the data is in transition (t_{DBSH} = Time, Data Before SCLK High).

When implementing a SPI port, whether it is a dedicated hardware peripheral port, or a software implemented port using general purpose I/O (also known as *Bit-Banging*) the timing parameters given in Figure 4 must be met to ensure reliable communications. The clock set-up and hold times, t_{DBSH} and t_{DASH} must be greater than 100 nS.

Idle Mode

The PNI 11096 does not initialize in the idle mode at power-up. The PNI 11096 must be in a data-ready state for the idle mode to occur. After power-up the PNI 11096 can be brought to the data-ready state by following these steps for sending a read command to the PNI 11096.

1. Set SSNOT low.
2. Pulse the RESET line.
3. Send a command to the PNI 11096 to measure one of the sensors.
4. Once the SSNOT pin is set to high again the PNI 11096 will go into the low power idle mode.
5. The DRDY pin will eventually go high signifying that the PNI 11096 is in the data-ready state. The resultant data *does not* have to be read from the PNI 11096.

Magnetic Measurements

The magnetic sensor operates in an oscillator circuit composed of the external bias resistors along with digital gates and a comparator internal to the PNI 11096. Only one sensor can be measured at a time. To measure a sensor, send a command byte to the PNI 11096 through the SPI port specifying the sensor axis to be measured. After dividing by the ratio set by PS2. PS1, and PSO, the PNI 11096 will return the result of a complete forward and reverse bias measurement of the sensor in a 16-bit 2's compliment format. The range is –32768 to 32767.

Command Byte

The operation of the PNI 11096 is controlled by the data received into the SPI port. The command byte syntax is as follows:

Table 9. Command Byte Syntax

Position	7	6	5	4	3	2	1	0
Bit	DHST	PS2	PS1	PS0	ODIR	MOT	ASI	ASO
RESET	0	0	0	0	0	0	0	0

AS0 and AS1 Axis Select Determines which axis is being measured.

N O T E When 2 MHz scaling is selected, the magnetic sensor oscillator does not run. Instead, the internal 2 MHz oscillator is turned on. The 2 MHz clock cycles are counted until a command byte is sent disabling the scaling function. A RESET stops the 2 MHz oscillator and clears all bits.

Table 10. AS0 and AS1 Axis Select

Function	AS1	AS0
2 MHz scaling	0	0
X axis	0	1
Y axis	1	0
Z axis	1	1

MOT
Magnetic Oscillator Test When set, causes the magnetic oscillator selected by AS0 and AS1, in the directions selected by ODIR to run continuously until PNI 11096 is reset.

ODIR
Oscillator Direction Determines the magnetic oscillator direction if MOT is set to 1. It has no effect on direction when the MOT bit is set to zero. *This is used for debug purposes only, and will not be set in normal operation.*

PS0, PS1, and PS2
Period Select Selects the division ratio applied to the L/R oscillator output to set the period being measured.

Table 11.

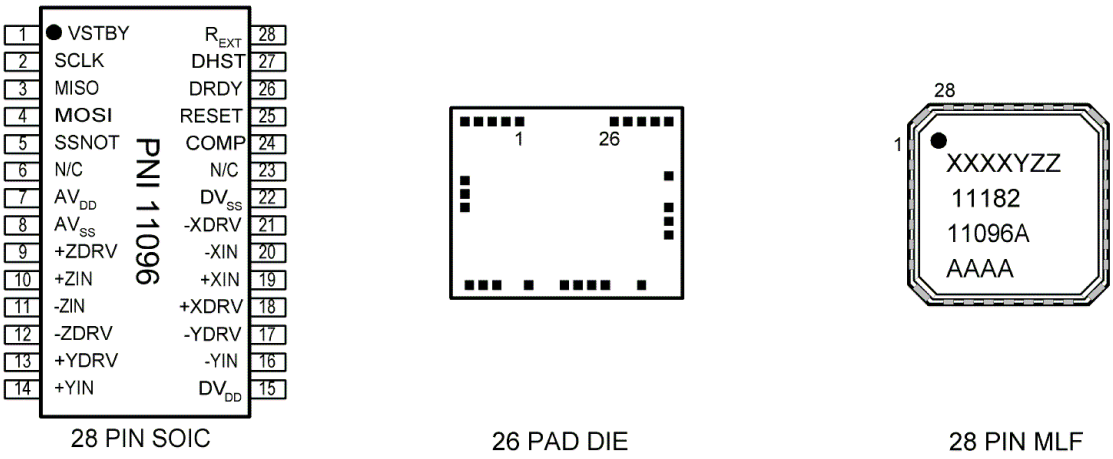
PS2	PS1	PS0	Ratio
0	0	0	/32
0	0	1	/64
0	1	0	/128
0	1	1	/256
1	0	0	/512
1	0	1	/1024
1	1	0	/2048
1	1	1	/4096

DHST
High Speed Oscillator Test When high, the internal high speed clock is set to drive the DHST pad at ½ the clock speed. When low, the DHST pad is set to DVDD. *This is used for debug purposes only, and will not be set in normal operation.*

Package Information

Pin Configuration

Figure 5. Pin Configuration



28 Pin SOIC Outline Dimensions

(Unit : mm)

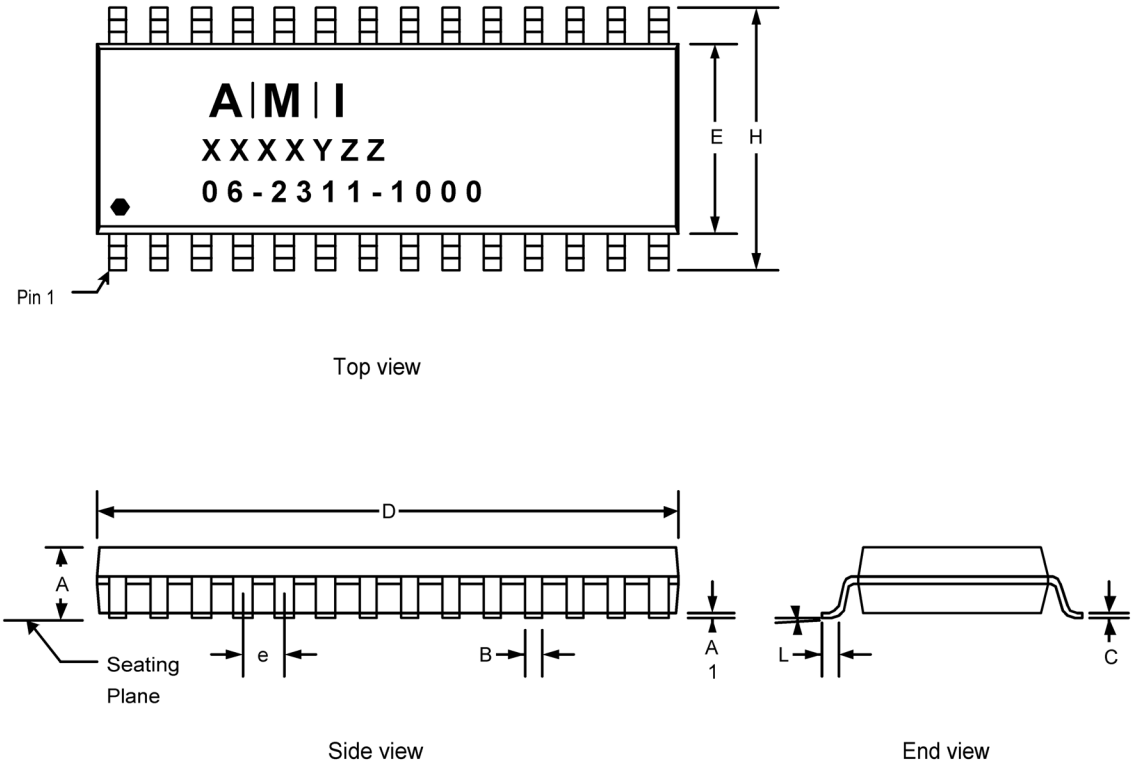


Figure 6. 28 Pin SOIC

Table 12. 28 Pin SOIC Outline Dimensions

Symbol	Minimum	Nominal	Maximum
A	2.35 mm		2.65
A1	0.10 mm		0.30 mm
B	0.33 mm		0.51 mm
C	0.23 mm		0.32 mm
D	17.70 mm		18.10
E	7.40 mm		7.60 mm
e		1.27 BSC	
H	10.0 mm		10.65 mm
L	0.40 mm		1.27 mm
α	0 mm		8 mm

28 Lead MLF (5 x 5 mm) Outline Dimensions

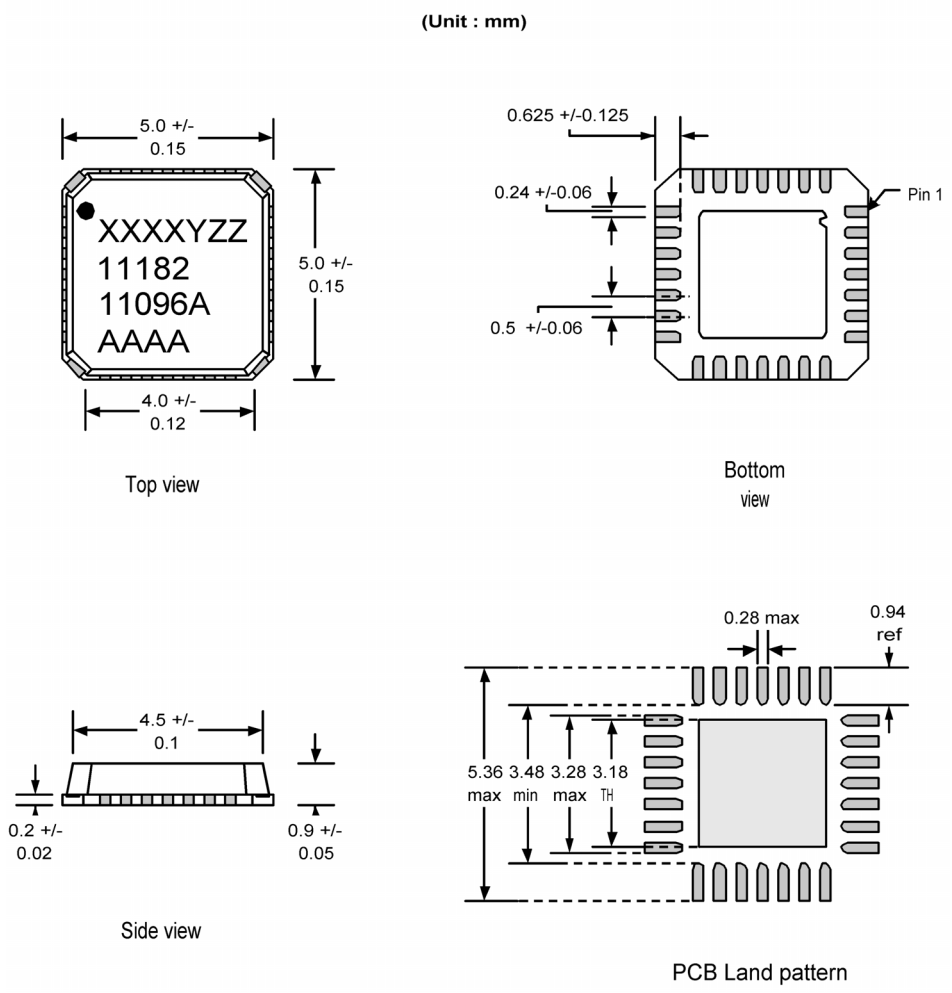


Figure 7. 28 Lead MLF (5 x 5 mm) Outline Dimensions

Die Package Mechanical Specifications

Die size is 2580 µm x 2360 µm (with scribe line). All X and Y coordinates refer to the center of the die.

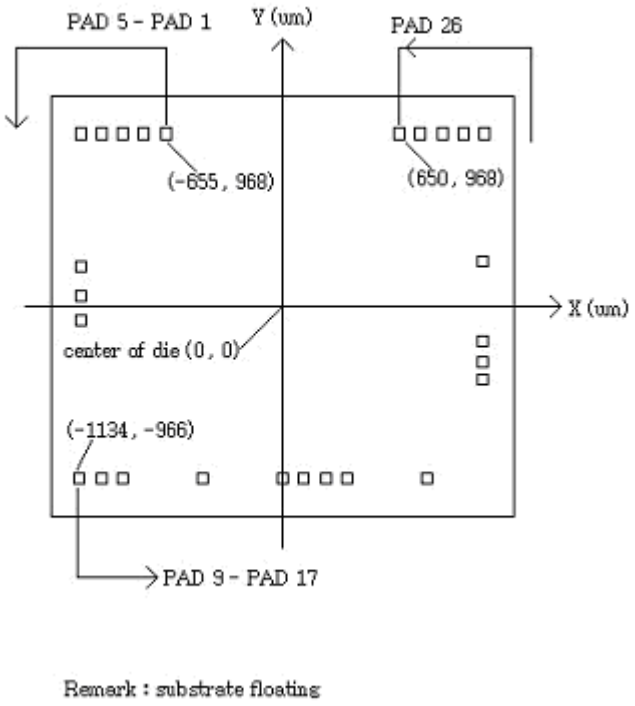


Figure 8. Mechanical Specifications

Table 13. Pad Descriptions

Pad	Function	X (μm)	Y (μm)
1	VSTBY	–655	968
2	SCLK	–755	968
3	MISO	–893	968
4	MOSI	–1012	968
5	SSNOT	–1128	968
6	AVDD	–1125	226
7	AVSS	–1125	62
8	APZDRV	–1125	–81
9	APZIN	–1134	–966
10	ANZIN	–1012	–966
11	ANZDRV	–893	–966
12	APYDRV	–448	–966
13	APYIN	–3	–966
14	DVDD	115	–966
15	ANYIN	237	–966
16	ANYDRV	357	–966
17	APXDRV	802	–966
18	APXIN	1118	–403
19	ANXIN	1118	–312
20	ANXDRV	118	–189
21	DVSS	1118	225
22	COMP	1126	968
23	RESET	1008	968
24	DRDY	887	968
25	DHST	768	968
26	REXT	650	968